Universidad Nacional Autónoma de México
FACULTAD DE INGENIERIA

DISEÑO Y CONSTRUCCION DE UN SISTEMA AUTOMATICO EXPERIMENTAL PARA ADQUISICION REMOTA DE DATOS HIDROLOGICOS

Tesis para obtener el Título de
INGENIERO MECANICO ELECTRICISTA
P r e s e n t a d a p o r:
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I N D I C E

1. INTRODUCCION

Los datos que se conocen acerca del clima (precipitación media anual, temperatura media anual, presión, humedad, cantidad de agua en los ríos, etc.) de una determinada región, son tomados de estaciones metereológicas. Estas se encuentran diseminadas en puntos estratégicos de la región en estudio. En ellas se encuentran instrumentos como pluviómetro, barómetro, anemómetro, veleta, etc. Para conocer las condiciones climatológicas de la región, es necesario que una persona vaya periódicamente a esas estaciones a tomar la lectura de los dispositivos. Esta es una labor difícil ya que la mayoría de las estaciones se encuentran en lugares apartados de la civilización y en lugares agrestes de difícil acceso.

De todo lo anterior surge la idea de construir una estación de campo (estación metereológica) que opere en forma automática, es decir, que la lectura de los diferentes dispositivos sea hecha en forma automática y que estos datos sean obtenidos en otro lugar lejano de las estaciones, pero cercano o en la civilización, ya sín la necesidad de que una persona tenga que ir al lugar a hacer este trabajo. Se tendría así un sistema de telemetría.

A finales de 1978, el Instituto de Ingeniería llevó a cabo un proyecto de desarrollo de una red telemétrica para previsión de avenidas para la presa Chicoasén, Chis.

Se tenía la necesidad de saber, en cualquier momento, el regimen pluviométrico de la región y a la vez el caudal que lleva el o los ríos que desembocan en la presa, para con-

esos datos poder predecir (mediante modelos de lluvia-escurrimiento) una posible avenida en la presa y poder así tomar las medidas precautorias necesarias.

El objetivo de este trabajo es el de realizar un sistema de medición similar al de Chicoasén, pero con técnicas digitales, con transmisión de datos en forma periódica. Para ello se penso en tecnologías CMOS y microprocesadores.

El sistema que se ideó está detallado en el diagrama de bloques de la fig. 1.

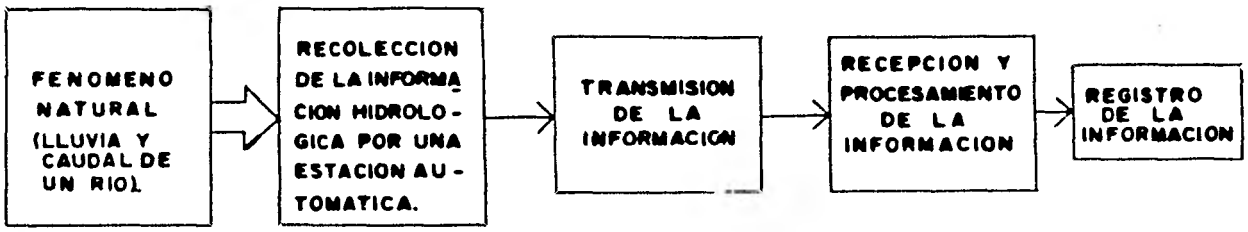


Fig. 1 Diagrama de bloques del sistema de adquisición remota de datos hidrológicos.

En el capítulo dos se detalla el diseño de un prototipo digital de estación de campo hecho con lógica alambrada, utilizando para ello circuitos integrados CMOS (Complementary Metal Oxide Semiconductor).

Con la experiencia adquirida con el prototipo hecho con lógica alambrada se procedió a diseñar otro prototipo que es manejado por un microprocesador. En el capítulo tres se describe el programa y la circuitería necesaria para que el microprocesador simule las actividades que realiza el autómata anterior.

Para complementar el diseño de este sistema de adquisición de datos, en el capítulo cuatro se describe el prototipo de la estación receptora que recibe y procesa la información proveniente de la estación de campo.

Una vez concluido el diseño y la construcción de este prototipo, surge la inquietud de posibles cambios y adaptaciones al sistema. Por tal motivo se presenta en el capítulo cinco una perspectiva de desarrollo de este sistema.

Finalmente en el capítulo seis se dan las conclusiones a las que se llegó después de haber probado en condiciones reales a estos prototipos.

2. ESTACION EXPERIMENTAL DIGITAL I: LOGICA ALAMBRADA

2.1 DESCRIPCION GENERAL

En la fig. 2 se muestran esquemáticamente las partes de la estación digital experimental de campo.

La transferencia de datos, desde la estación remota- se lleva a cabo mediante un enlace de radio VHF calidad voz.- La estación de campo opera en forma intermitente con período- programable y consta de dos fases: conteo y transmisión. Durante la primera, el transmisor está apagado y se cuentan los eventos de precipitación del pluviómetro tipo balancín (0.25mm de lluvia por evento). La segunda fase se inicia activando - el transmisor, enviando la información de precipitación acumulada durante el intervalo anterior junto con un identificador de estación; se desactiva el transmisor y se inicia una nueva fase de conteo.

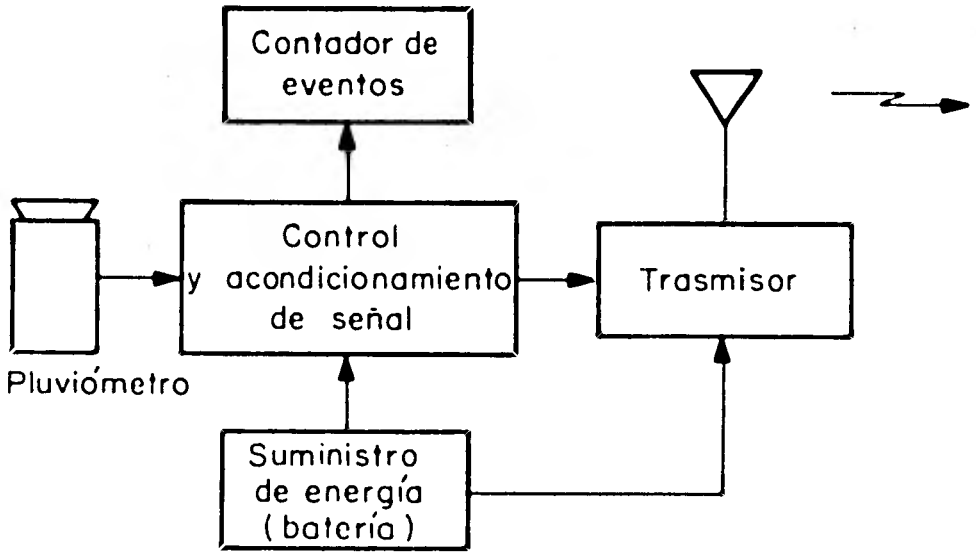


Fig. 2 Estación de Campo

Los datos se transmiten en forma seriada con modulación FSK a 110 bauds.

2.2 CIRCUITOS EN LA ESTACION DE CAMPO

2.2.1 DIAGRAMA DE BLOQUES

Este se muestra en la fig. 3. Se estructuró el circuito con un bus paralelo de 8 bits. Sobre este bus se depositan ordenadamente (uno a la vez) los datos del identificador de estación programado y posteriormente los del contador de eventos de precipitación. Por su flexibilidad, esta estructura permitirá agregar otro datos paralelos como pudiesen ser

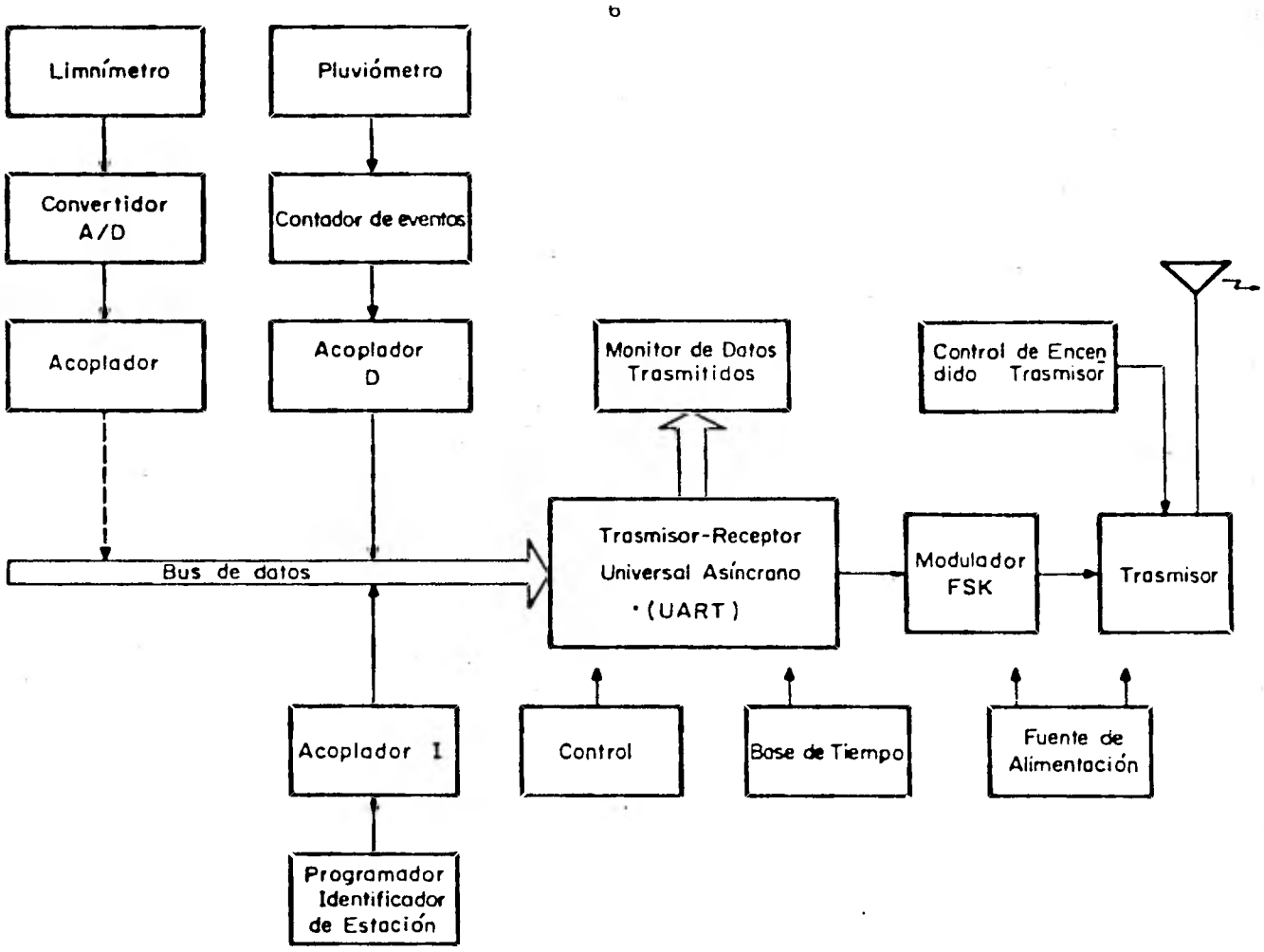


Fig. 3 Acondicionador de señal en la estación de campo

los de un limnímetro, termómetro, etc.

La información del bus se serializa y codifica con un UART (receptor-transmisor universal asíncrono) y el tren de pulsos a su salida se acondiciona y modula mediante FSK para su transmisión a través de un canal radiofónico.

Un circuito de control fija la frecuencia de acceso al bus de los diferentes dispositivos y controla el encendido del transmisor y el inicio de transmisión de datos.

Con la base de tiempo se controlan los períodos de transmisión y recolección de datos.

Mediante un monitor visual, se pueden verificar los datos transmitidos.

A continuación se describen con detalle cada parte del circuito de la estación de campo, haciendo referencia al diagrama electrónico de la fig. 4.

2.2.2 BASE DE TIEMPO Y RELOJ

Esta etapa genera la señal excitadora para la sección de control. A partir de un oscilador a cristal de 2.01 MHZ (fig. 4) se divide la frecuencia entre 2^{21} mediante el circuito IC1 obteniendo una señal Ⓐ con frecuencia $f_2 = 0.957$ HZ y período $t_2 = 1.045$ seg. Con su flanco de bajada se excitan los circuitos IC2 e IC13. IC2 es un contador binario de 7 etapas, con el cual, al dividir entre 2^6 (64) se obtiene una señal con $f_3 = 1.5 \times 10^{-2}$ HZ y $t_3 = 66.6$ seg. (aprox. 1 minuto) y al dividir entre 2^4 (16) da $f_4 = 5.98 \times 10^{-2}$ HZ y $t_4 = 16.7$ seg. Estas dos señales se observan en los puntos de prueba TP2' y TP2", respectivamente.

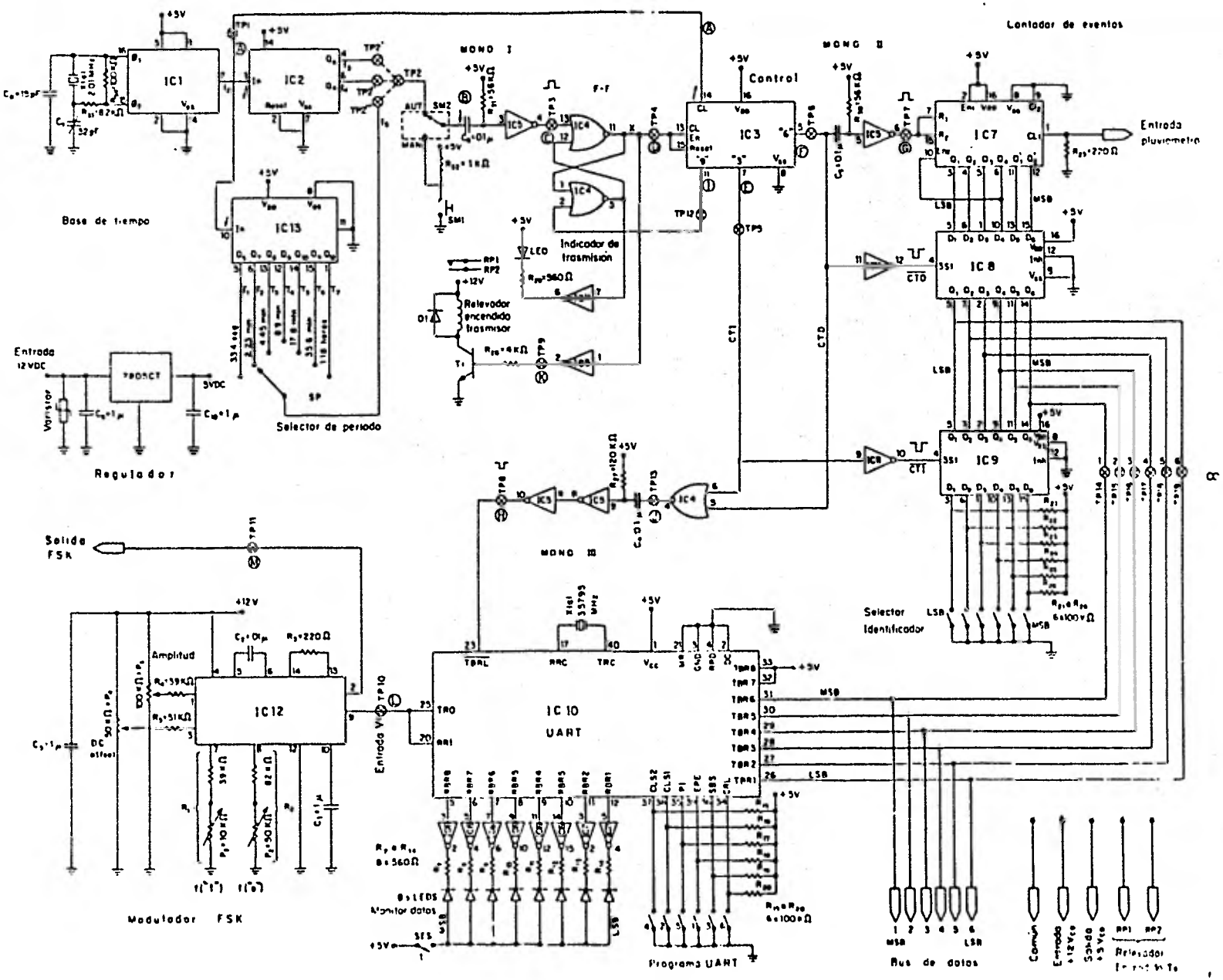


Fig. 4 Acondicionador de señal en la estación de campo

El circuito IC13 es un contador binario de 14 etapas del cual, a partir de f_2, se obtienen 7 señales:

$f_6 = 2.99 \times 10^{-2}$ HZ, $t_6 = T_1 = 33.44$ seg
$f_7 = 7.47 \times 10^{-3}$ HZ, $t_7 = T_2 = 133.86$ seg = 2.23 min
$f_8 = 3.73 \times 10^{-3}$ HZ, $t_8 = T_3 = 4.45$ min
$f_9 = 1.865 \times 10^{-3}$ HZ, $t_9 = T_4 = 8.92$ min
$f_{10} = 8.9325 \times 10^{-3}$ HZ, $t_{10} = T_5 = 17.84$ min
$f_{11} = 0.4662 \times 10^{-3}$ HZ, $t_{11} = T_6 = 35.68$ min
$f_{12} = 0.2331 \times 10^{-3}$ HZ, $t_{12} = T_7 = 71.36$ min

Con el selector SP, pueden seleccionarse cualquiera de las señales anteriores y observarse en el punto de prueba TP2''' (f_5).

Finalmente, mediante un puente de TP2', TP2" o TP2''' hacia el punto TP2, pueden escogerse las frecuencias fijas f_3 y f_4, o una frecuencia variable f_5. Como se verá posteriormente, estas frecuencias fijarán el período de las fases de recolección (conteo) y transmisión de datos de la estación de campo.

2.2.3 CONTROL

La sección de control esta compuesta por los circuitos MONO I, F-F, IC3, MONO II, IC5, y MONO III (fig. 4).

Opera impulsada por la señal Ⓑ, que llega del selector SM2. Con él se escoge el modo de operación: AUT, automático controlado por la base de tiempo y MAN, iniciando una transmisión manualmente con SM1.

El flanco negativo de la señal Ⓑ inicia en ambos - casos el envío de datos.

La operación de la sección de control se explicará - con base en la fig. 4 y el diagrama de impulsos de fig. 5.

El flip-flop con las compuertas NOR de IC4 y el contador IC5 forman un circuito monoestable digital que genera - la señal Ⓚ de encendido del transmisor y los pulsos para - transferencia del identificador y datos Ⓔ y Ⓕ respectivamente.

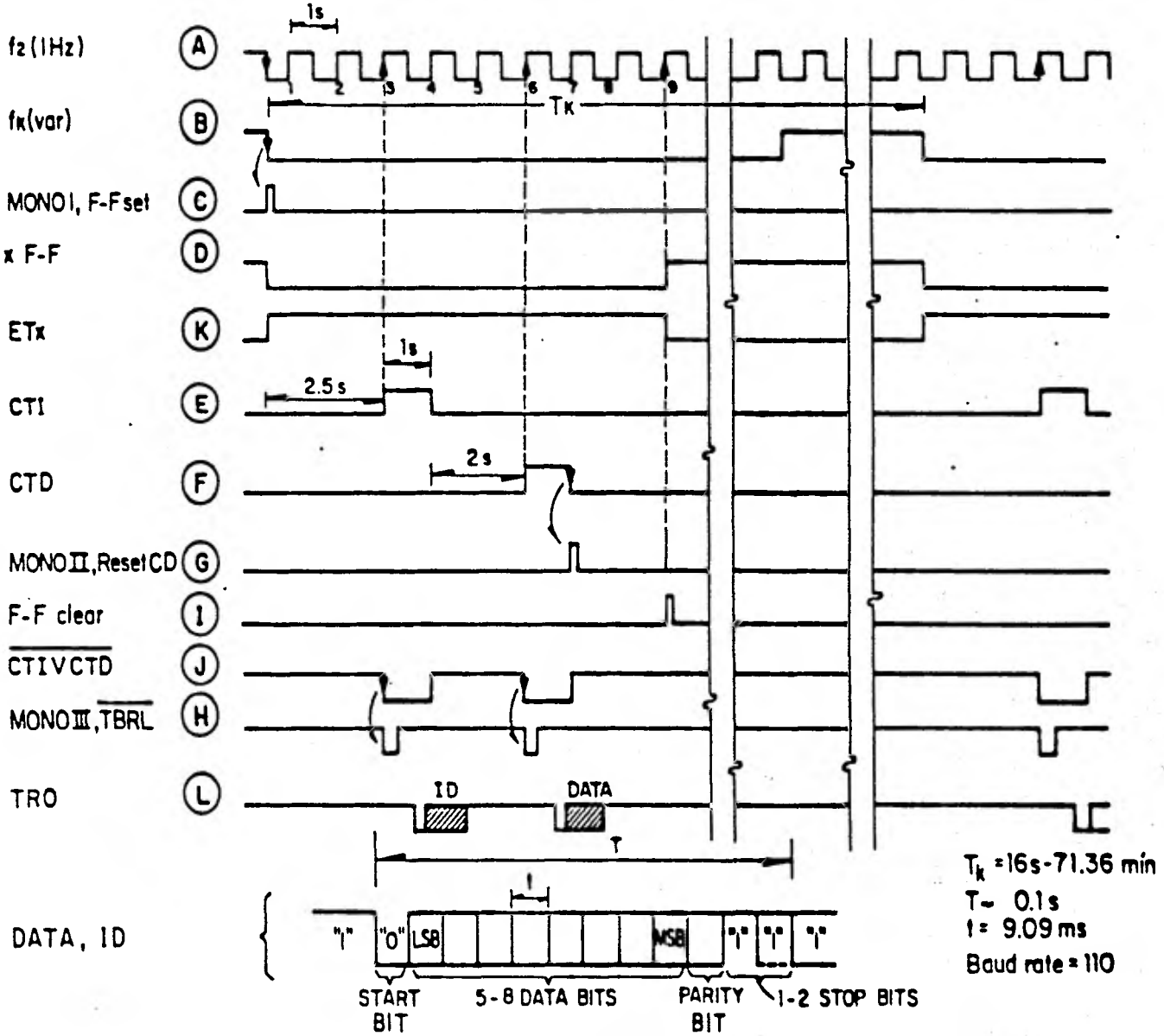
Con el flanco negativo de Ⓑ se genera un pulso Ⓒ - de 5 mseg con el monoestable MONO I que pone al flip-flop. Su salida Ⓓ, normalmente en "1" baja a "0" y habilita al contador de década tipo Johnson IC3 que comienza a contar a razón- de f_2 = 1 HZ (señal Ⓐ).

A su vez la señal Ⓓ se invierte con IC5 Ⓚ y a - través de T_1 y un relevador enciende el transmisor (cierra su circuito de alimentación con RP1 y RP2).

El contador de década IC3 tiene sus salidas decodificadas a decimal. Cuando llega a la cuenta de 3 (3 seg) genera en su correspondiente salida un pulso Ⓔ (CTI) que se emplea para la transferencia de los datos del identificador del bus. Al mismo tiempo esta señal dispara a través de IC4 al monoestable MONO III que inicializa con Ⓗ ($\overline{\text{TERL}}$) la serialización- mediante IC10 (UART) de los datos del bus (en este instante - los del identificador).

De manera semejante la señal Ⓕ (CTD) al cabo de - una cuenta de 6 seg de IC3, habilita la transferencia de los- datos del contador de eventos al bus y el inicio de su seria-

Fig. 5 Diagrama de impulsos



lización por IC10 con la señal (H).

Con el flanco negativo de (F) (CTD) se dispara el monoestable MONO II que pone a cero con (G) al contador de even-- tos para iniciar un nuevo ciclo de conteo de datos del pluviómetro.

Con la cuenta "9", señal (I), de IC3, se cierra el ciclo poniendo a cero el flip-flop, inhibiendo el contador IC3- (poniendolo a cero) y apagando el transmisor.

Termina así la fase de serialización y transmisión - de datos, que comenzará nuevamente con el siguiente flanco - negativo de (B). Con IC11, conectado al flip-flop, se enciende un LED como indicador de transmisión durante el tiempo en- que permanece prendido el transmisor.

Si se quisiera expander el circuito para incorporar- los datos de un limnímetro al bus y transmitirlos (fig. 3), - bastará ampliar el contador IC3 con otro en cascada, y con - una de sus salidas agregar a la secuencia de datos por transmitirse la del tirante del río, antes de cerrar con el pulso- (I) en el ciclo de transmisión.

2.2.4 CONTADOR DE EVENTOS

Los eventos de precipitación registrados por el pluviómetro (cierre de un interruptor por cada 0.25 mm de llu- - via) son contados y almacenados por IC7, un contador binario- de 8 bits. Las salidas de este contador quedan conectadas - a través del acomplador IC8, que tiene salidas "tri-state", - al bus de datos. Por simplicidad sólo se alambraron 6 líneas del bus (6 bits). Estas pueden observarse en los puntos de - prueba TP14-TP19.

Las salidas de IC8 normalmente se encuentran en estado de alta impedancia, excepto cuando aparece el pulso Ⓕ - - (CTD), durante el cual se transfieren los datos del contador- al bus.

2.2.5 GENERADOR DEL IDENTIFICADOR DE ESTACION

Esta sección emplea el circuito IC9, idéntico a IC8, y un grupo de selectores para programar el identificador de - la estación. La transferencia desus datos al bus se controla con la señal Ⓔ (CTI) de igual manera que con el contador de - eventos.

2.2.6 UART

El receptor-transmisor universal asíncrono, compuesto por IC10 (IM 6403 IPL), serializa los datos paralelos del bus agregando automáticamente bits de inicio, paridad y finalización. Mediante 6 selectores se programa al UART para el formato de datos deseado, es decir, número de bits de datos, definalización y tipo de paridad.

En la fig. 5 se muestra el bloque de información que ensambla el UART.

La duración de cada bit, así como la velocidad de - transmisión 110 bauds son controlados internamente en el circuito a partir de su propia base de tiempo mediante un cris-- tal de 3.57954 MHZ.

Los datos ensamblados y serializados aparecen en la- salida Ⓛ (TRO). Con el pulso Ⓗ ($\overline{\text{TBRL}}$) se inicia la transmi-- sión de cada dato presente en el bus.

Para esta aplicación se programó el UART para transmitir 8 bits, aunque el bus sea de 6. Los dos bits más significativos se pusieron en "1".

2.2.7 MONITOR DE DATOS

Para visualizar y verificar los datos serializados y transmitidos, se empleó la sección de recepción del mismo UART, conectando la salida Ⓘ (TRO) a la entrada del receptor-RRI. Este convierte nuevamente los datos de serie a paralelo. A través de IC6 e IC11 se invierten estos datos y se visualizan con LEDS.

Para inhibir la operación (consumo de energía) del monitor se abre el interruptor SES1.

2.2.8 MODULADOR FSK

Con él se acondicionan los datos digitales del UART para el medio de transmisión, en este caso radioenlace FM, calidad voz.

El modulador FSK (modulación por desplazamiento de frecuencia) se realizó con base en el circuito IC12 (XR2206), que es un generador de funciones.

Las frecuencias para los dos estados lógicos están dados por:

$$f("1") = \frac{1}{R_1 C_2} \qquad f("0") = \frac{1}{R_2 C_2}$$

y se escogieron como:

$$f("1") = 2400 \text{ HZ} \qquad f("0") = 1200 \text{ HZ}$$

Su ajuste se efectúa con los potenciómetros P_3 y P_2 respectivamente.

El modulador entrega a su salida una señal senoidal Ⓜ con baja distorsión, cuya amplitud se ajusta con P_5 y su nivel de CD con P_4. La impedancia de salida es 600 ohm.

Este circuito es el único que requiere alimentación +12 VDC.

2.2.9 REGULADOR DE TENSION

El suministro de energía para la estación de campo es de +12 VDC que se toma de una batería automotríz en flotación con un cargador.

Esta tensión se emplea en el modulador FSK y en el relevador para el encendido del transmisor. El transmisor también opera con +12 VDC.

Todo los demás circuitos digitales requieren +5 VDC que se toman de un regulador 7805 (IC14).

Para protección de los circuitos se conectó a la línea de +12 VDC un varistor para suprimir posibles transitorios en la alimentación.

2.2.10 ESPECIFICACIONES TECNICAS DE LA ESTACION DE CAMPO

Función:	Recolección y transmisión digi-- tal de datos hidrológicos.
Modo de operación:	Intermitente periódico. Ciclo de 2 fases: conteo y transmisión. - Operación manual o automática.
Medio de transmisión:	Canal radiofónico, compatible - con línea telefónica.
Transductor:	Pluviómetro tipo balancín, 0.25 mm de lluvia por descarga (even- to), interruptor de mercurio pa- ra registro local y telemetría.
Registro locaL:	Contador electromecánico, +12 - VDC para registrar precipitación total acumulada.
Perído de transmisión:	Variable: 16.7 seg, 33.4 seg, - 1.1 min, 2.23 min, 4.45 min, - 8.92 min, 17.84 min, 35.68 min,- 71.36 min.
Duración de la transmisión:	8.5 seg: datos 4 seg, encendido- transmisor 2.5 seg antes y 2 seg después de datos.
Codificación de los datos:	Paquete de dos datos: identifica dor de estación y precipitación- acumulada. Formato tipo ASR-33, 110 bauds: Start bit, 5-8 data - bits, parity bit, 1-2 stop bits.
Identificador de estación:	Programable mediante microin- - terruptores.

Acondicionamiento de datos:	Modulación FSK, nivel alto 2400-HZ, nivel bajo 1200 HZ, amplitud ajustable: 0.2-6 Vp-p, nominal - 1.2 Vp-p.
Imedancia de salida señal FSK:	600 ohms
Monitores:	8 LEDS para dato transmitido, 1-LED para encendido transmisor.
Equipo de comunicación:	Transmisor "Repco", VHF, - 166.69008 MHZ, FM, 2.2 watt, calidad voz, operación intermitente, 12-15 VDC. Antena tipo Yagi, VHF de 5 elementos.
Suminiestro de energía - eléctrica:	Cargador y batería tipo automotríz en flotación, +12 VDC.
Consumo de corriente:	Fase de conteo (transmisor y monitor datos apagado): 20.7 mA; - fase de transmisión: tarjeta - 79mA, transmisor 400 mA. Consumo total promedio con T = 8.92 - min: 21.7 mA. Vcc = +12 VDC.
Voltaje de alimentación:	Tarjeta: 10.5 - 18 VDC, regulador interno a + 5 VDC.
Protecciones:	Pararrayos con electrodo a tierra. Supresor de transitorios DC.
Electrónica:	Digital, CMOS, sobre tarjeta de-circuito impreso.
Temperatura de operación:	+ 5°C a 45°C.

3. ESTACION EXPERIMENTAL DIGITAL II: MICROPROCESADOR

3.1 DESCRIPCION GENERAL

En esta parte se presenta la segunda alternativa de-realización para la recolección de datos hidrológicos. Dado-al advenimiento tecnológico de los microprocesadores, se procedió a desarrollar un sistema como el que se muestra en el - diagrama de bloques de la fig. 6.

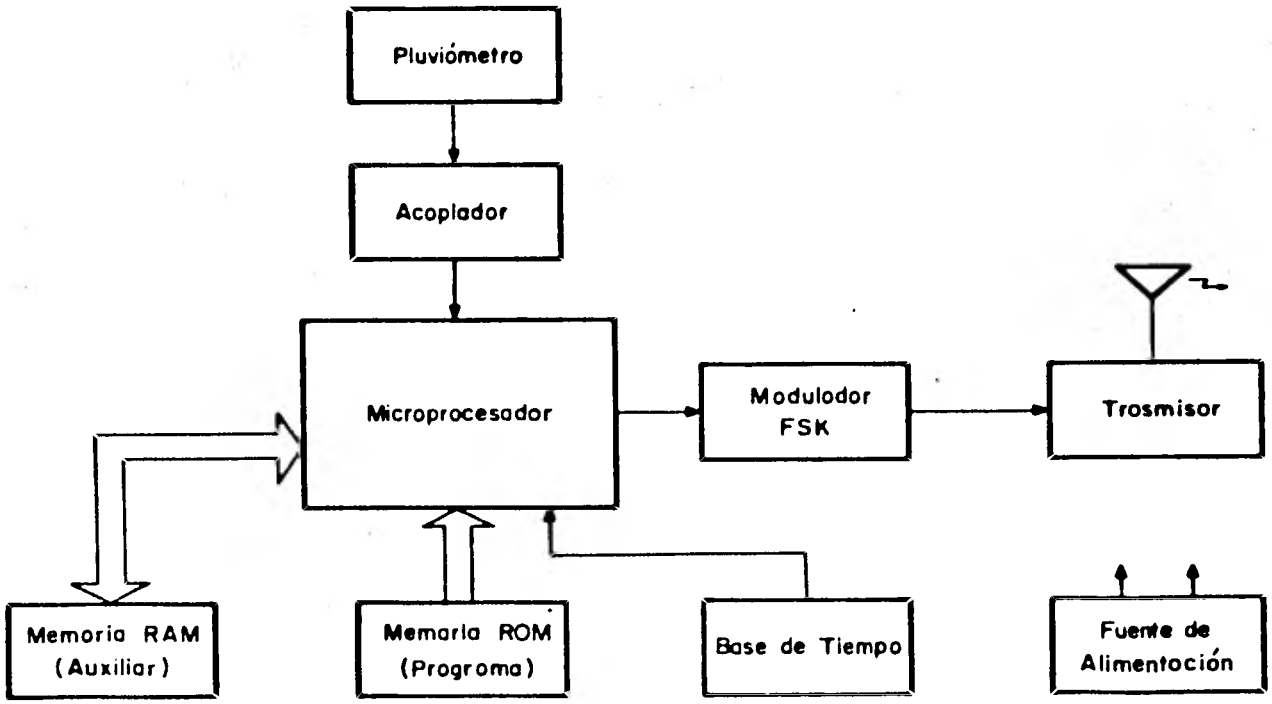


Fig. 6 Estación de campo

Como se observa, la estación de campo se realizó alrededor de un microprocesador (SC/MP-I). Este controla el ciclo de trabajo de la estación mediante un programa almacenado permanentemente en memoria no volátil PROM.

La medición de precipitación se efectúa nuevamente mediante un pluviómetro tipo balancín, que acciona un interruptor cada vez que se acumulan 0.25 mm de lluvia.

Este evento (cierre del interruptor) se registra y almacena en forma incremental en memoria, acumulándose la precipitación hasta el inicio de la fase de transmisión.

Con la base de tiempo del micrprocesador (1 MHZ) y subrutinas de retardo se controlan los períodos de recolección y transmisión de datos. Al iniciarse el período de transmisión de datos, se enciende el transmisor y se envían los datos. Para ello, por programa se serializan, codifican y acondicionan mediante modulación FSK y se transmiten a 110 bauds.

El transmisor es de VHF, con modulación FM, calidad-voz. El suministro de energía eléctrica es mediante un cargador y batería automotríz en flotación.

La estación opera en dos modos: automático y manual. En el primero (fig. 7), al darse un reset el programa entra al período de recolección de datos.

Durante Tmax se cuentan los eventos del pluviómetro y al final de éste se transmite el paquete de información, y se repite nuevamente el ciclo.

En el modo manual (fig. 7), después del reset se transmite inmediatamente la información que se tenga acumula-

da y al término de esta transmisión empieza el período de recolección de datos, siguiendo, a partir de este momento, el modo de transmisión automático.

3.1.1. DESCRIPCION DEL MICROPROCESADOR SC/MP

Para realizar el sistema descrito en el diagrama de-bloques de la fig. 6 se escogió el microprocesador SC/MP de - National Semiconductor Co.

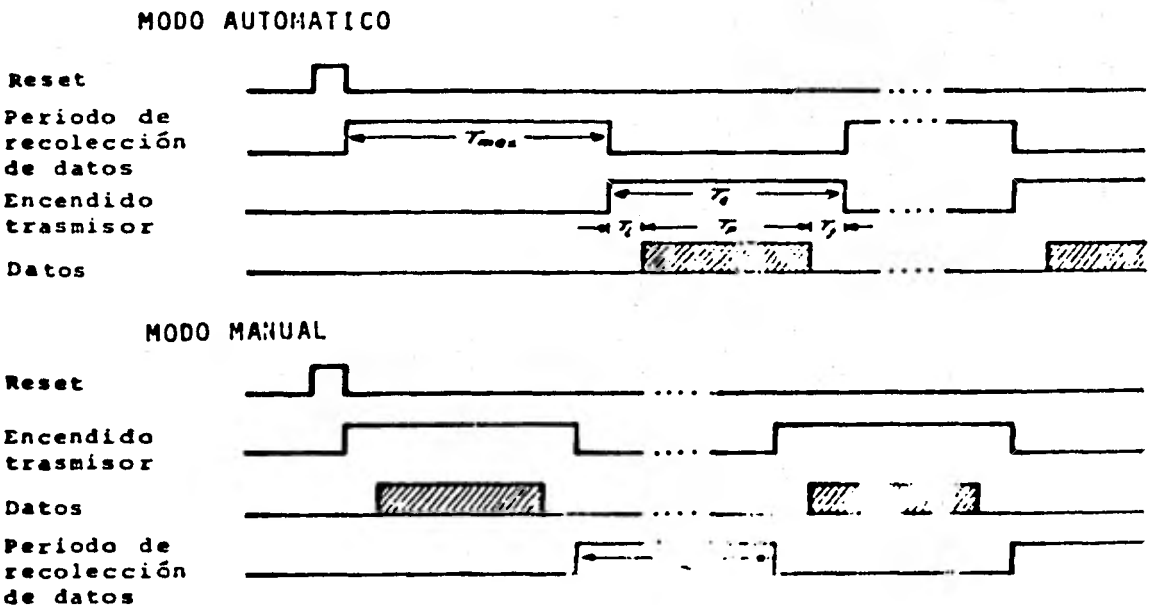


Fig. 7 Diagrama de tiempos

El SC/MP es un microprocesador de 8 bits que esta - contruido en un solo circuito integrado, con tecnología MOS - (Metal Oxide Semiconductro) canal P de empobrecimiento. La - arquitectura de su unidad central de procesamiento (CPU) se -

muestra en la fig. 8.

Este microprocesador cuenta con un acervo de 46 instrucciones; entre ellas, operaciones lógicas, aritméticas, manejo de registros y acceso directo a memoria (DMA). Tiene una capacidad de direccionamiento de hasta 65 536 localidades de memoria.

Por software se pueden controlar interrupciones, señales de control de entrada/salida (comunicación con dispositivos externos) y transferencia de datos en serie o en paralelo.

Además puede ser conectado a circuitos TTL (Transistor Transistor Logic) o CMOS sin problema de acomplamiento (ver los circuitos equivalentes de los manejadores y receptores del SC/MP en las hojas de especificaciones en el Apéndice A).

3.2 CICLO DE TRABAJO

Como se mencionó en el subcapítulo 3.1, las actividades que se llevan a cabo en la Estación Experimental II siguen un determinado orden y a un determinado tiempo. Esta secuencia de actividades esta controlada por el microprocesador, mediante el programa CONPLU I (Contador del Pluviómetro). El diagrama de flujo simplificado de este programa se muestra en la figura 9.

Al darse un reset, todos los registros del microprocesador se borran y empieza a correr el programa almacenado en PROM (memoria programable de sólo lectura). Este programa comienza su operación con la sección de INICIACION; en esta parte se pone a cero la memoria (flip-flop) que "atrapa" el

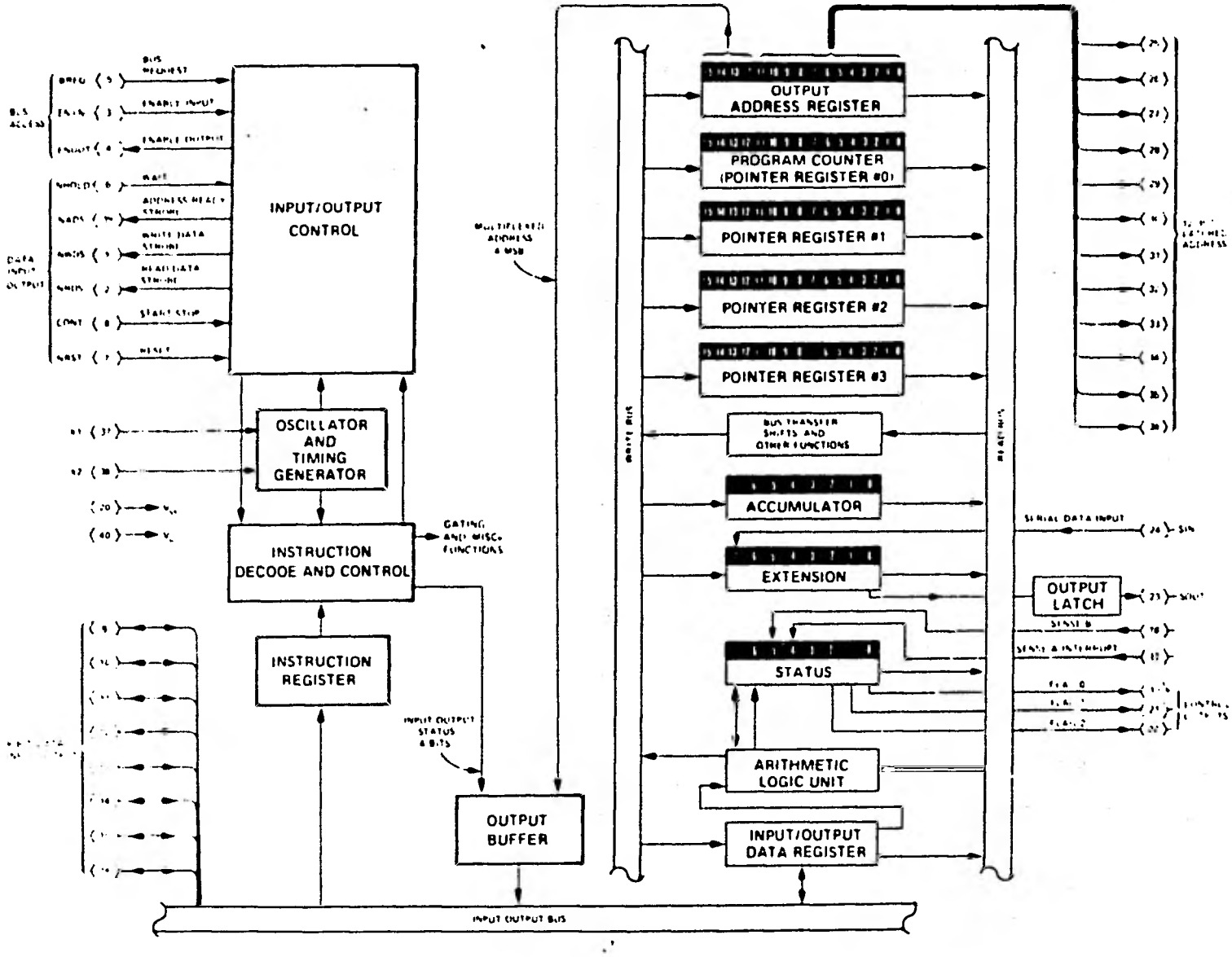


Fig. 8 Arquitectura del CPU del SC/MP

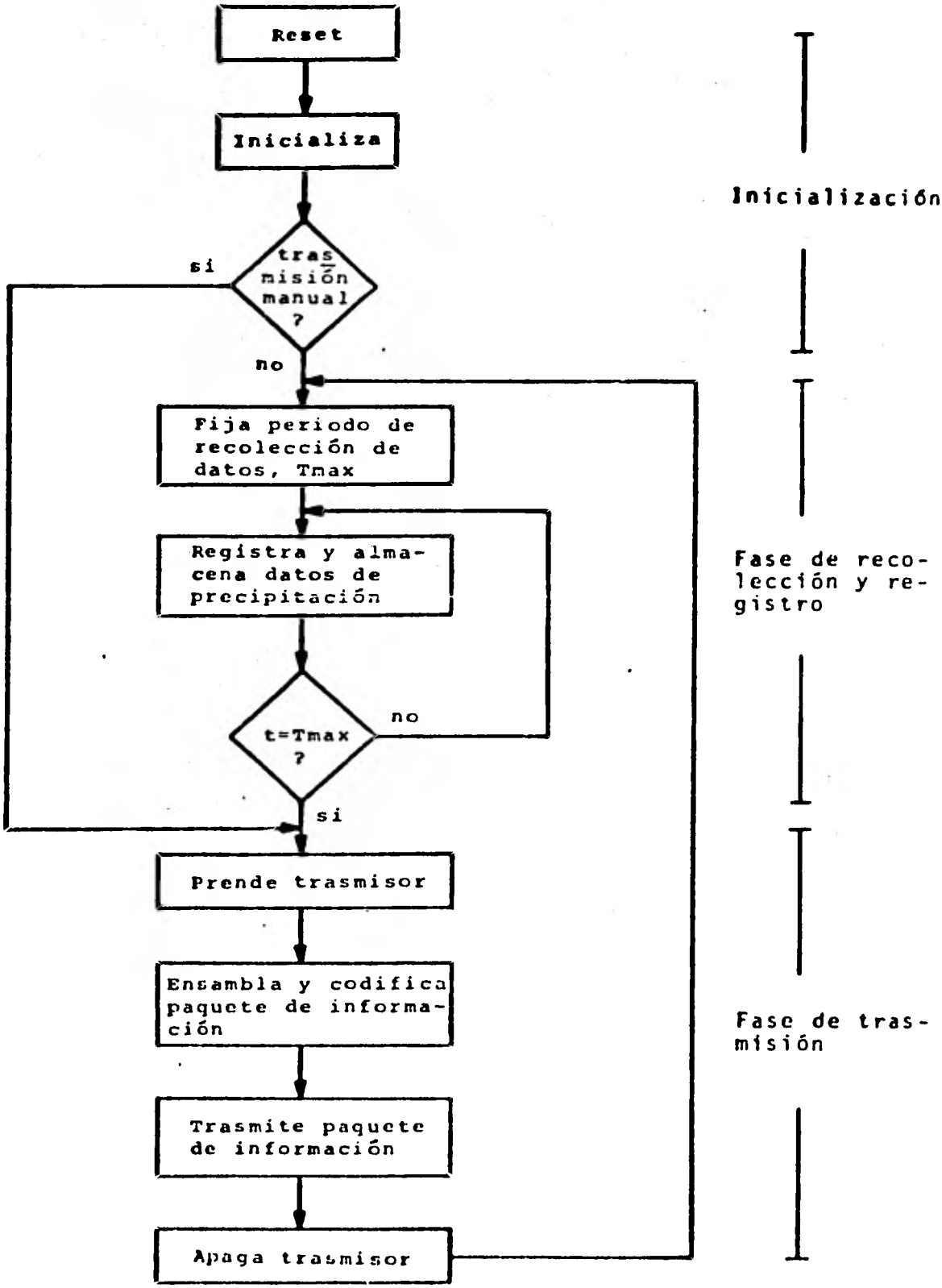


Fig. 9 Ciclo de trabajo

pulso proveniente del pluviómetro y se analiza si la operación va a ser manual o automática. El modo de operación se escoge previamente con un selector conectado a uno de los circuitos receptores del microprocesador (Sense B fig. 8).

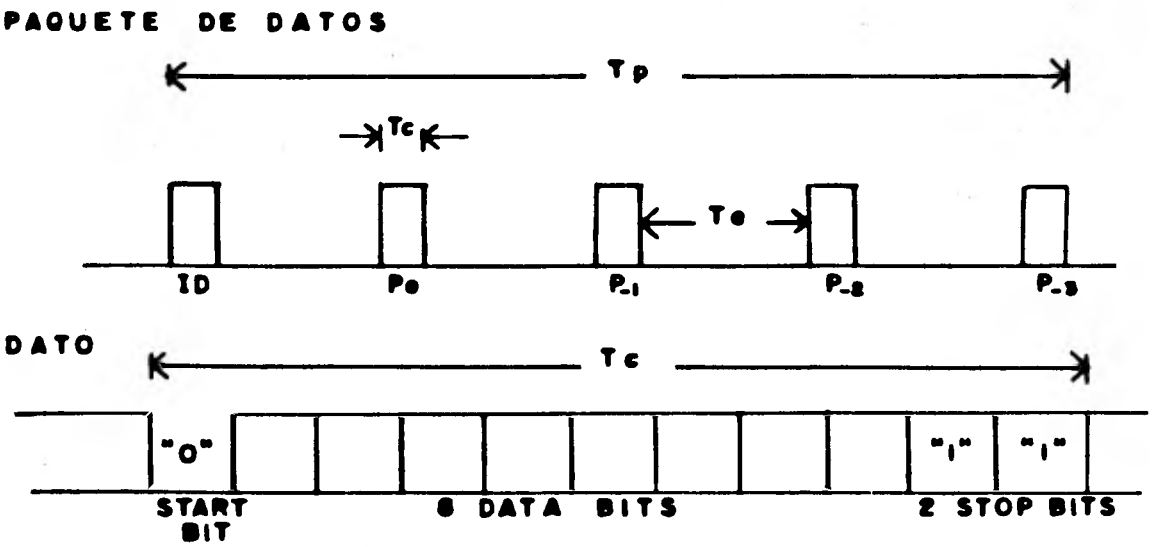
Si el modo de transmisión es manual se transmite inmediatamente la información que se tiene en los registros de datos (Po, P_{-1}, P_{-2}, y P_{-3}). Para ello, por programa se analiza la línea sensora B, si su estado es alto, significa que el operador quiere que se transmita inmediatamente la información acumulada hasta ese momento.

Si el estado de la línea sensora B es bajo significa que la operación es automática normal. En este modo se alternan periodicamente las fases de recolección y transmisión.

La fase de recolección y registro se compone de una rutina de retardo que fija el tiempo, (Tmax) de recolección de datos (10 minutos típico); esta rutina es interrumpida con la llegada de cada evento (pulso) del pluviómetro. Este pulso pone en alto la salida de un flip-flop conectada a la línea sensora A del microprocesador, que al detectar un estado alto provoca una interrupción en el programa. Con la interrupción se pasa a la subrutina de conteo donde se incrementa en una unidad la localidad de memoria de la precipitación total acumulada (Po) y se regresa a la rutina de retardo.

Transcurrido el tiempo programado para la recolección y registro de eventos se procede a la transmisión de la información. Para ello es necesario abrir primero el canal de transmisión. Esto se logra alimentando al transmisor con un voltaje de +12 VDC a través de un relevador, activado a su vez por un transistor manejado por el microprocesador utilizado el "latch" de salida S10 del registro de extensión (ver fi

gura 8). La información consiste en un paquete de 5 datos codificados (figura 10) formado por: identificador de la estación ID, precipitación total acumulado Po y tres datos redundantes con la precipitación acumulada de tres períodos anteriores P_{-1}, P_{-2} y P_{-3}.



Tp = 2.5 seg
Tc = 0.1 seg
Te = 0.5 seg

Fig. 10 Formato de transmisión

La conversión a serie y transmisión de los datos se lleva a cabo por programa a diferencia de la versión con lógica alambrada, en la cual se empleaba un UART. El dato a transmitir se carga al registro de extensión y se saca, mediante corrimientos hacia el Flag 0 y de allí al modulador FSK para su acondicionamiento. La velocidad de transmisión es de 110 bauds.

Cada dato consta de un bit de inicio, 8 bits de información y dos bits de finalización. Enviado el paquete de datos seriados se apaga el transmisor, se reacomodan los registros de las precipitaciones acumuladas para la próxima transmisión y se inicia nuevamente la fase de recolección y registro.

La redundancia en la transmisión de datos permite a la estación de registro recobrar la información en caso de pérdida durante alguna transmisión.

El listado de este programa se encuentra en el apéndice B.

3.3 CIRCUITOS ELECTRONICOS DE LA ESTACION CON MICROPROCESADOR

Con el programa anterior (3.2) se le dan al microprocesador una serie de instrucciones a seguir, para que ejecute una secuencia de actividades en la estación de campo. Algunas de estas actividades son inherentes al microprocesador (conteo de pulsos, retardos, etc.), pero otras (encendido del radio, modulación de la información, etc.). deben ser realizadas por dispositivos externos al microprocesador. Estos se describirán a continuación.

La estación de campo consta de dos tabletas de circuito impreso (fig. 11): una corresponde al propio microprocesador y la otra a todos los circuitos auxiliares.

3.3.1 CIRCUITO IMPRESO DEL MICROPROCESADOR Y SUS COMPONENTES.

Sobre la tarjeta del microprocesador se encuentra, además del chip ISP 8/500D (microprocesador), una memoria EPROM (MM5204 Q) que contiene al programa (CONPLU), memoria RAM (dos chips MM2101 - 1D), un buffer inversor (SN 7414N),

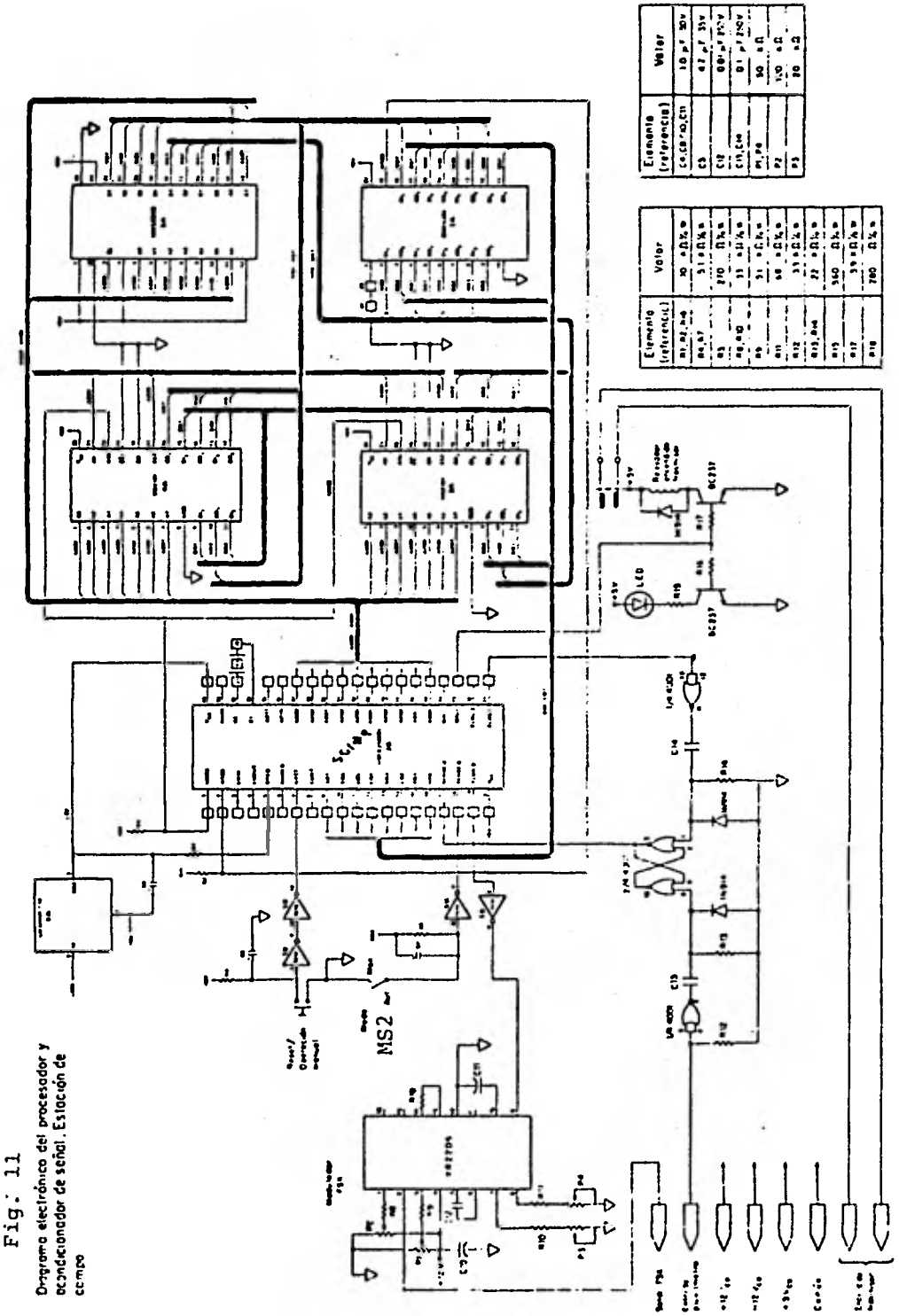


Fig. 11

Programa electrónico del procesador y acondicionador de señal. Estación de campo

un buffer "tri-state" para el bus de datos (DM 81LS95 N), un- regulador de voltaje (LM 320 MP) y un cristal de 1.0 MHZ - (Y1).

3.3.2 CIRCUITO DEL RESET Y SELECTOR DEL MODO DE OPERACION

El punto de partida de la operación de la estación - de campo se da al dar un reset al microprocesador. El circuito (ver fig. 11) consiste en un "push-button" (normalmente - abierto) y dos inversores en serie (no inversión) conectados- al pin 7 (NRST) del microprocesador. En operación automática normal el pin 7 debe tener un estado alto. Cuando se oprime el "push-button" se presenta en el pin 7 un estado bajo, du-- rante el cual se aborta el programa en proceso. Al retornar- al estado alto ("push-button" libre) una circuitería interna- del microprocesador borra todos los registros accesibles al - programador y trae la primera instrucción que se encuentra en la localidad 0001 HEX. El circuito RC funciona como un amortiguador para absorber los rebotes que se provocan al oprimir el "push-button".

Una vez dado el reset, el programa "pregunta" si la- transmisión va a ser manual o automática. Esta "pregunta" se hace detectando la señal que esté presente en el pin 18 - (Sense B fig. 11), del chip del microprocesador. Para ello - se tiene un micro-interruptor N (MS2) y un inversor; con este arreglo se puede presentar al pin 18 un estado bajo (transmisión automática) dejando el interruptor abierto, y un estado- alto (transmisión manual) cerrando el interruptor a tierra.

Esto significa que previamente al reset debe escoger se el modo en que va a operar la estación. Si se escoge el - modo de operación manual (MS2 cerrado) significa que cada vez que se de un reset la estación transmitirá inmediatamente los datos acumulados hasta ese momento.

3.3.3 ACOPLADOR PLUVIOMETRO-MICROPROCESADOR

El pluviómetro mide la precipitación mediante un balancín, el cual al captar 0.25 mm de lluvia acciona momentáneamente un interruptor. Este interruptor esta conectado en serie con una batería de +12 VDC y con un contador eléctromecánico (fig. 12). Al cerrarse el interruptor se permite el paso de corriente hacia la bobina del contador, aumentando en una unidad su cuenta. La finalidad de este contador es la de registrar localmente los eventos. Así mismo el pulso de +12 VDC se reduce a uno de 5V mediante un diodo Zener para ser compatible con el microprocesador.

El pulso es "atrapado" dentro por un circuito Flip-Flop (fig. 11). El "Set" (Entrada Pluviómetro) de este Flip-Flop (F/F) lo da el pluviómetro y el "Reset" lo da el microprocesador (Flag 1).

Este arreglo es accionada por los flancos de bajada de los pulsos en S y en R, es decir, cuando desaparece el pulso proveniente del pluviómetro, la salida (pata 3 del chip 4001) se pone en alto y es puesta en un estado bajo con el flanco de bajada del pulso que manda el microprocesador.

La salida del F/F está conectada a la pata 17 (sense A) del microprocesador y además es la entrada de interrupción del programa en operación.

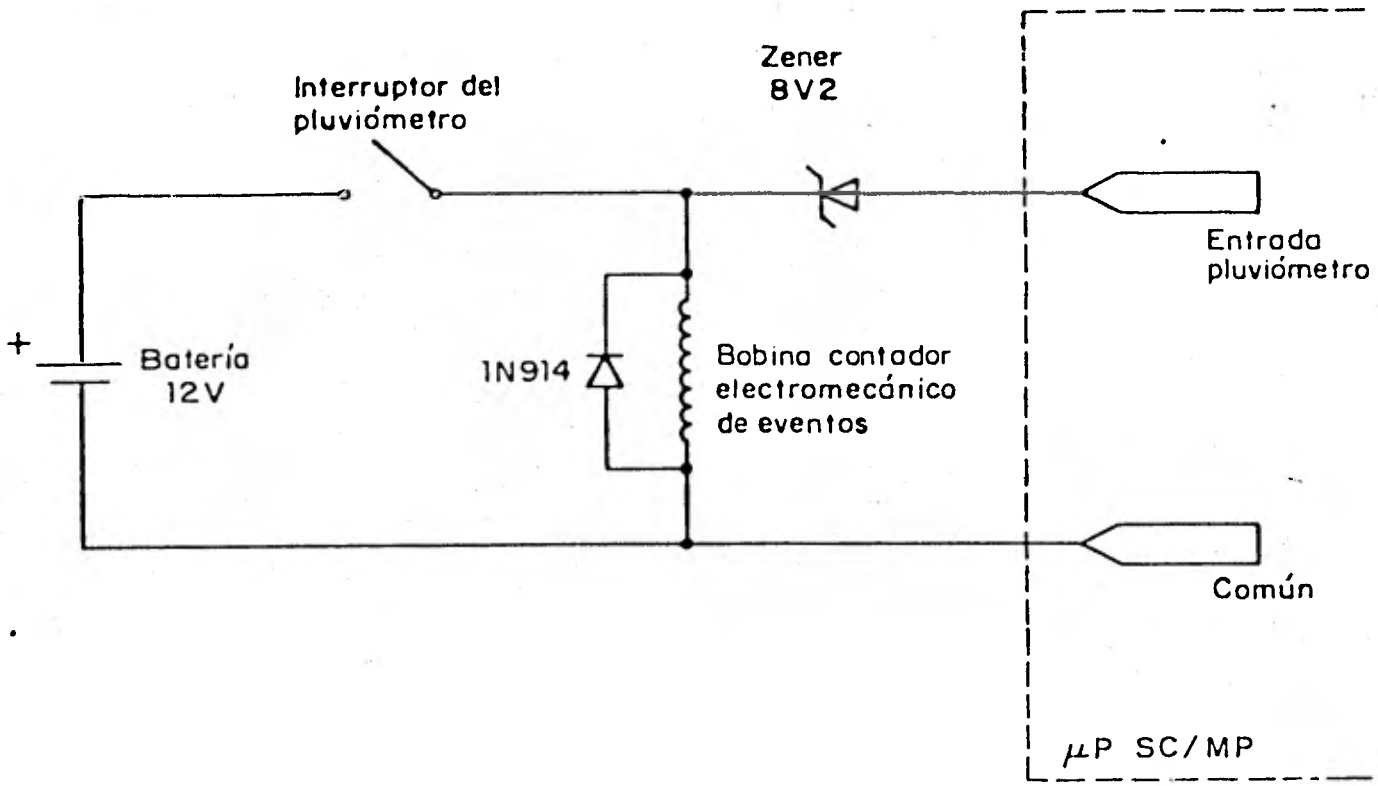


Fig. 12 Circuito Acoplador Pluviómetro MP SC/MP

Resumiendo, la secuencia de eventos se da de esta manera: aparece el pulso del pluviómetro y pone un estado alto en la salida del F/F, el programa detecta este estado, lo registra y pone un estado bajo al F/F.

3.3.4 ENCENDIDO DEL TRANSMISOR

Como se mencionó anteriormente (3.2) se requiere prender el transmisor antes de transmitir el bloque de datos y apagarlo después del envío del mismo. Para ello se tiene un relevador que permite el paso de corriente al transmisor

cada vez que se transmite.

En la fase de transmisión el programa utiliza la pata 23 (SOUT) del microprocesador para accionar el transistor BC237 que maneja al relevador. Al mismo tiempo que se acciona el relevador se prende un LED (Diodo Emisor de Luz) para monitorear el encendido del transmisor. Este LED permanece prendido durante 4.5 seg. que es el tiempo que permanece activo el radio enlace.

3.3.5 MODULADOR FSK

Para la transmisión del paquete de información se emplea la técnica FSK (Codificación por corrimiento de frecuencia). Para ello se utiliza un circuito integrado como generador FSK (XR2206 en la fig. 11). Para el nivel lógico "1" se asignó una frecuencia de 2400HZ y para el "0" 1200HZ.

Utilizando las fórmulas de diseño para este circuito se tiene:

$$f_{"1"} = 2400 = \frac{1}{R_X C}$$

y

$$F_{"0"} = 1200 \quad \frac{1}{R_Y C}$$

escogiendo C = 0.01 microfarad, y sustituyendo

$$R_x = R_{10} + P_3$$

$$R_y = R_{11} + P_4$$

en donde P_3 y P_4 sirven para el ajuste fino de las frecuencias respectivas.

Además se tienen los potenciometros P_1 y P_2 para dar el nivel de DC de la señal FSK y ajuste de la ganancia de la misma señal, respectivamente.

La señal FSK se alimenta al radio transmisor.

3.3.6 FUENTE DE ALIMENTACION

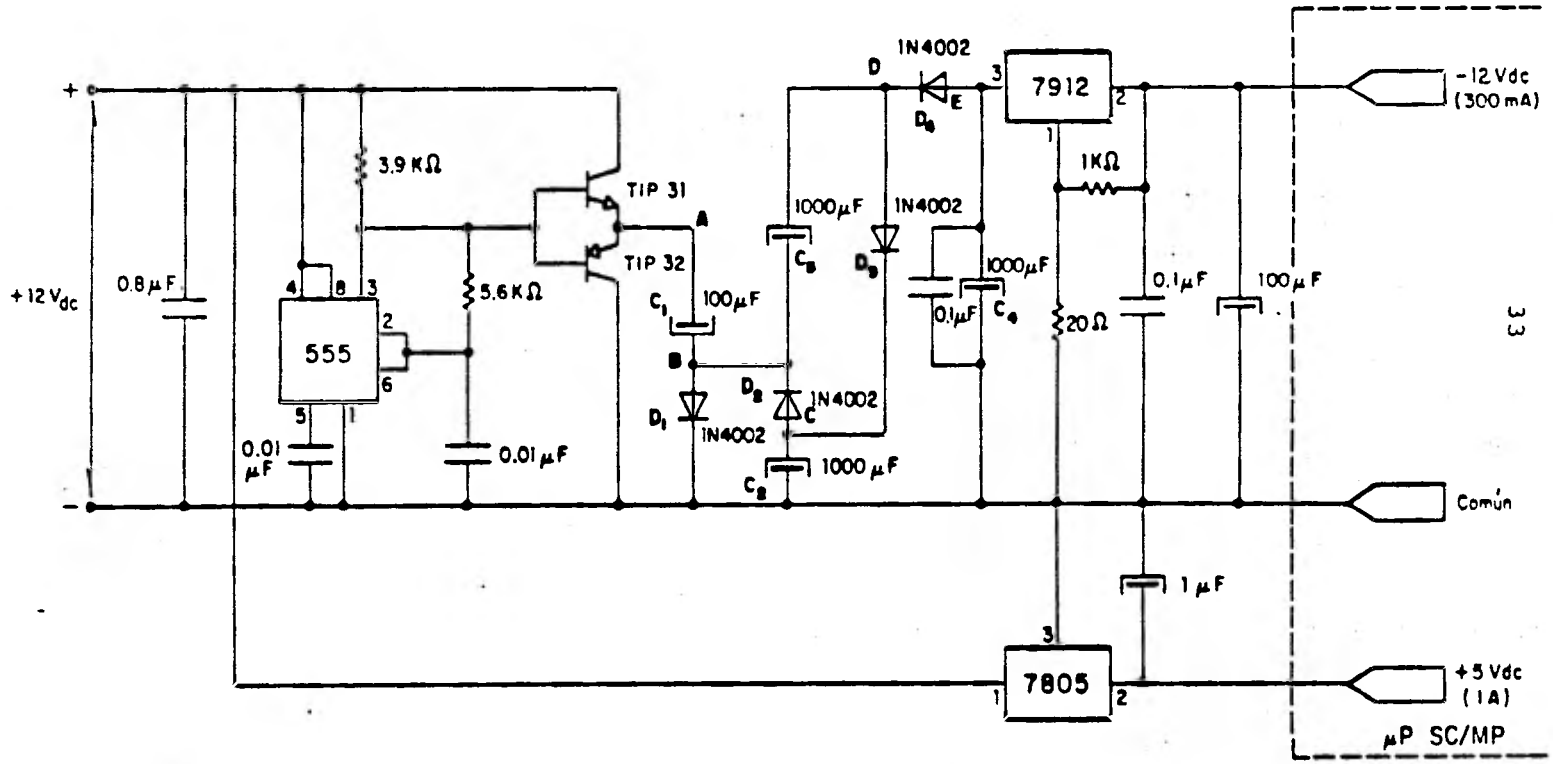
El suministro de energía en la estación de campo está dado por una batería automotríz (+12VDC) en flotación con un cargador (que puede ser un convertidor AC-DC o un panel de celdas solares). Ya que la tableta del microprocesador opera con +5VDC y -12 VDC y la tableta con la circuitería de soporte opera con +5 VDC y +12 VDC, es necesaria la conversaión de los +12 VDC de la batería a +5 VDC y -12 VDC. Esto se logra con el circuito mostrado en la fig. 13.

Este circuito convertidos de voltaje DC-DC contiene los siguientes circuitos integrados básicos: Un generador de pulsos (timer 555), dos transistores de potencia (TIP31 y TIP32), un regulador a +5 VDC (7805) y un regulador a -12 VDC (7912).

La salida (pata 3) del circuito 555, maneja a un amplificador de corriente (TIP31 y TIP32), cuya salida pasa a un circuito doblador de voltaje (formado por C_1, C_2, C_3 y C_4, D_1, D_2, D_3, y D_4). En la fig. 14 se muestran las formas de onda de las señales en los puntos A, B, C, D y E, el circuito opera así:

Cuando la salida A es alta, C_1 (B) se carga a través de D_1, D_2 no conduce. Cuando la salida A es baja, la carga de C_1 es transferida a C_2 (C) por medio de D_2, ya que D_1 queda polarizado en inversa. Cuando la salida A es otra vez

Fig. 13 Convertidor de +12 Vdc a −12 Vdc y +5 Vdc



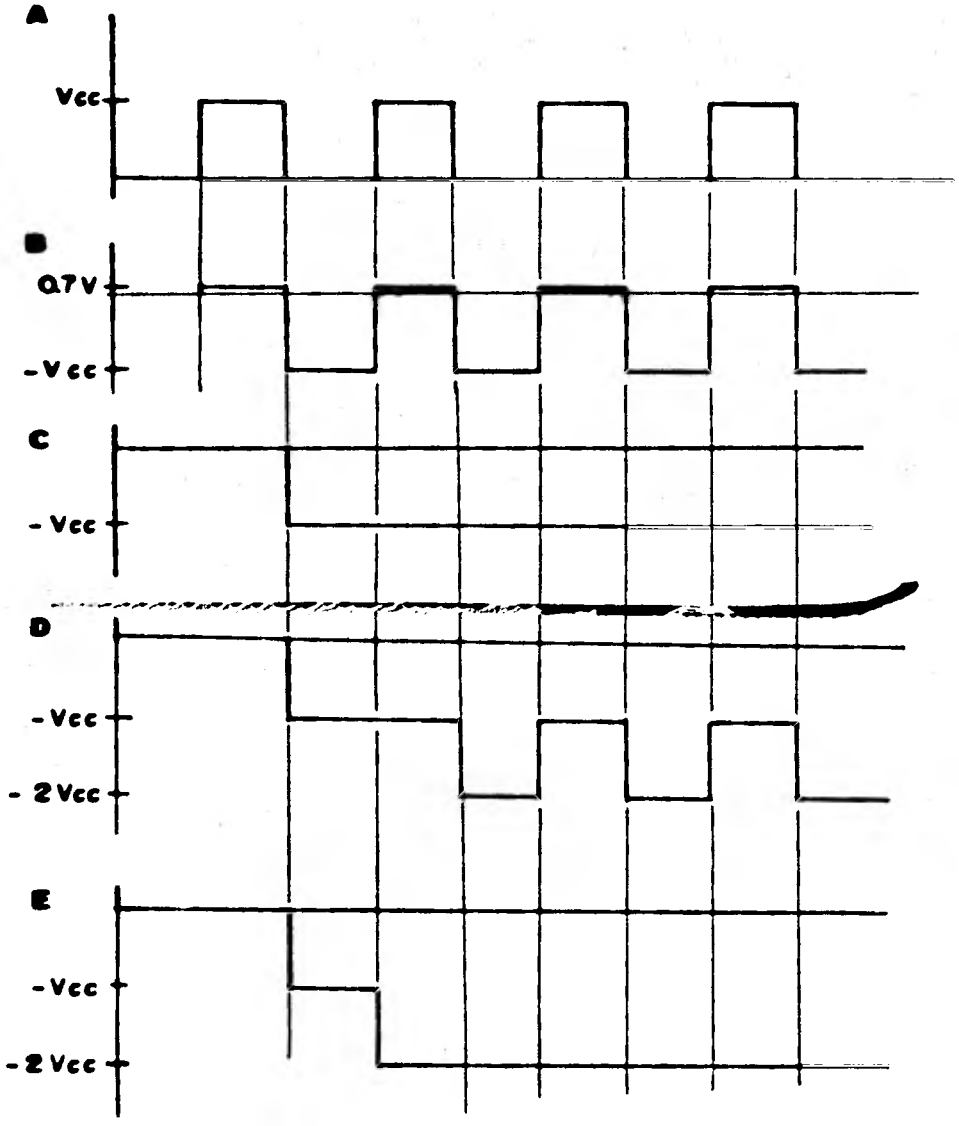


Fig. 14 Formas de onda (ideales) del circuito regulador de voltaje (-12 VDC)

alta, C_3 (D) es cargado por C_2 através de D_3 de tal manera - que en ese punto se tiene aproximadamente menos el voltaje - de alimentación (Vcc = 12VDC). Cuando A es otra vez bajo, la carga de C_3 (D) es transferida a C_4 (E) por medio de D_4 (D_1,- D_2, y D_3 no conducen), teniendose de esta manera dos veces - (aproximadamente) el voltaje de alimentación a la entrada - (pata 3) del regulador de voltaje.

En el nodo E se tiene conectado un circuito regula-- dor de voltaje (7912) con el cual, si en E se tienen variaciones de voltaje de $-2Vcc \angle E \angle -$ (Vcc +3), se puede asegurar que a la salida de este circuito integrado (pata 2) se tiene un voltaje constante de -12 VDC @ 300 mA.

Para el requierimiento de +5VDC se conectó a +12 VDC el regulador 7805 cuya salida (pata 2) tiene un voltaje constante de +5VDC @ 1 amp.

3.4 RADIOENLACE

En el prototipo descrito se utilizó un transmisor - de alta frecuencia (VHF), 2 Watts de potencia, con antena tipo Yagi de alta ganancia.

3.5 ESPECIFICACIONES TECNICAS DE LA ESTACION DE CAMPO

Función	Recolección y transmisión digi-- tal de datos hidrológicos.
Modo de operación:	Intermitente periódico. Ciclo de dos fases conteo y transmisión.- Operación manual o automática. - Transmisión asíncrona.
Transductor:	Pluviómetro tipo balancín, 0.25mm de lluvia por descarga (evento), interruptor de mercurio para re- gistro local y telemétrico.
Período de transmisión:	Fijo por programa. 10 minutos - típico.
Duración de la transmisión:	4.5 : Datos 3 segs. con 0.5 seg. entre dato y dato. Encendido - del transmisor 1 seg. antes y - 0.5 seg. después de datos.
Codificación de datos:	Paquete de 5 datos: Identifica-- dor de la estación, precipitación acumulada actual y precipitacio- nes acumuladas de tres transmi-- siones anteriores. Formato ASR-33 110 bauds: start bit, 8 data - bits, 2 stop bits.
Identificador de la esta- ción:	Fijo (EØ HEX) en el programa de- la memoria EPROM.
Acondicionamiento de datos:	Modulación FSK, nivel alto 2400- HZ, nivel bajo 1200 HZ, amplitud ajustable 0.5 a $6V_{pp}$, nominal - 1 V_{pp}.

Impedancia de salida. Señal FSK:	600 ohms.
Monitores:	LED para encendido de transmisor.
Equipo de comunicación:	Transmisor REPCO, VHF, 166.69008 MHZ, FM, 2 Watt, calidad voz, operación intermitente, 12-15 VDC. Antena Yagi, VHF de 5 elementos.
Suministro de energía eléctrica	Cargador y batería automotríz en flotación + 12 VDC.
Consumo de corriente:	Fase recolección de datos: 600 ma. aprox. Fase transmisión: 1 amp. aprox.
Voltajes de alimentación:	Batería, + 12VDC; convertidor de voltaje, - 12 VDC y + 5VDC.
Necesidades de voltaje:	Tableta, +12VDC y +5VDC; tarjeta microprocesador, +5VDC -12VDC; transmisor, +12VDC.
Protecciones:	Pararrayos con electrodos a tierra. Supresor de transitorios DC (en + 12VDC).
Electrónica:	Digital. Circuitos MOS, CMOS y TTL.

4. ESTACION DE REGISTRO

4.1 DESCRIPCION GENERAL

La estación de registro es la parte complementaria - del enlace telemétrico. En ella se recibe la señal de radiofrecuencia transmitida por la estación de campo, se decodifica y alimenta a un microcomputador, el cual interpreta y procesa la información.

El diagrama de bloques de la estación de registro se muestra en la fig. 15.

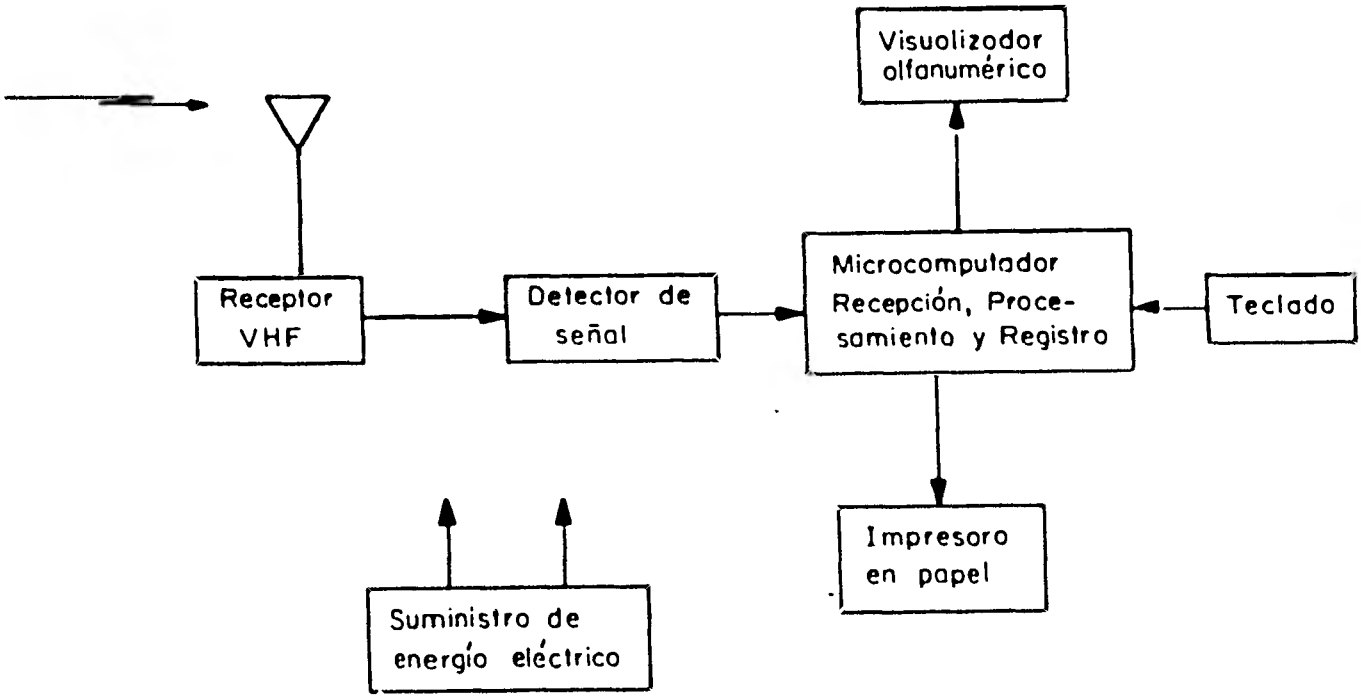


Fig. 15 Partes integrantes de la estación de registro.

4.2 DIAGRAMA DE BLOQUES

Como se muestra en el diagrama de la fig. 16 el equipo de la estación de registro se desarrolló alrededor del microcomputador AIM-65 de Rockwell. Por su versatilidad en cuanto a programación, registro y comunicación a un costo bajo, resultó propio para esta aplicación de adquisición de datos. Su diagrama funcional se muestra en la fig. 17.

En la estación de registro el receptor de VHF, continuamente encendido, detecta la señal de radio enviada por la estación de campo. Esta señal, modulada en FSK, primeramente se demodula y convierte a niveles lógicos apropiados. A su vez cada dato del paquete de información se detecta y decodifica por un receptor asíncrono (UART) programado para la velocidad y formato de transmisión empleado. Cada vez que recibe un dato correcto, lo convierte a paralelo y lo transfiere a un registro de salida junto con una señal de "dato recibido" (DR). Esta señal interrumpe al procesador, que ejecuta de inmediato una rutina de lectura y transferencia del dato del UART hacia memoria.

Recibido y almacenado el paquete de datos, se procesa y los resultados se registran permanentemente sobre papel junto con la estación, fecha y hora de recepción.

Durante el tiempo de espera se ejecuta un programa reloj fechador, cuyos datos se presentan actualizados en el visualizador alfanumérico. Mediante este programa se lleva control en tiempo del período de arribo de la información.

4.3 DIAGRAMA DE FLUJO DEL PROGRAMA

Un diagrama de flujo simplificado del programa para-

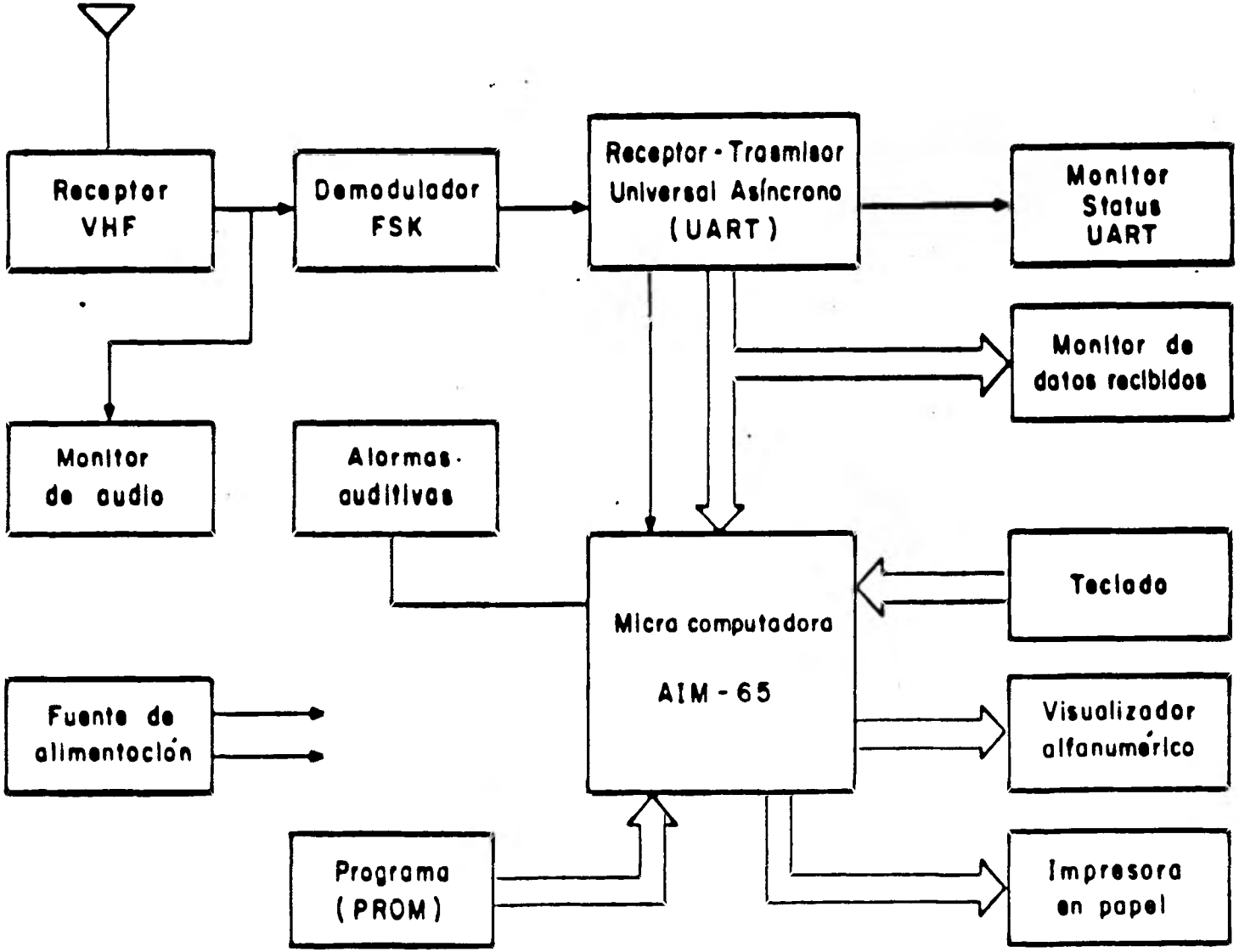


Fig. 16 Estación de registro

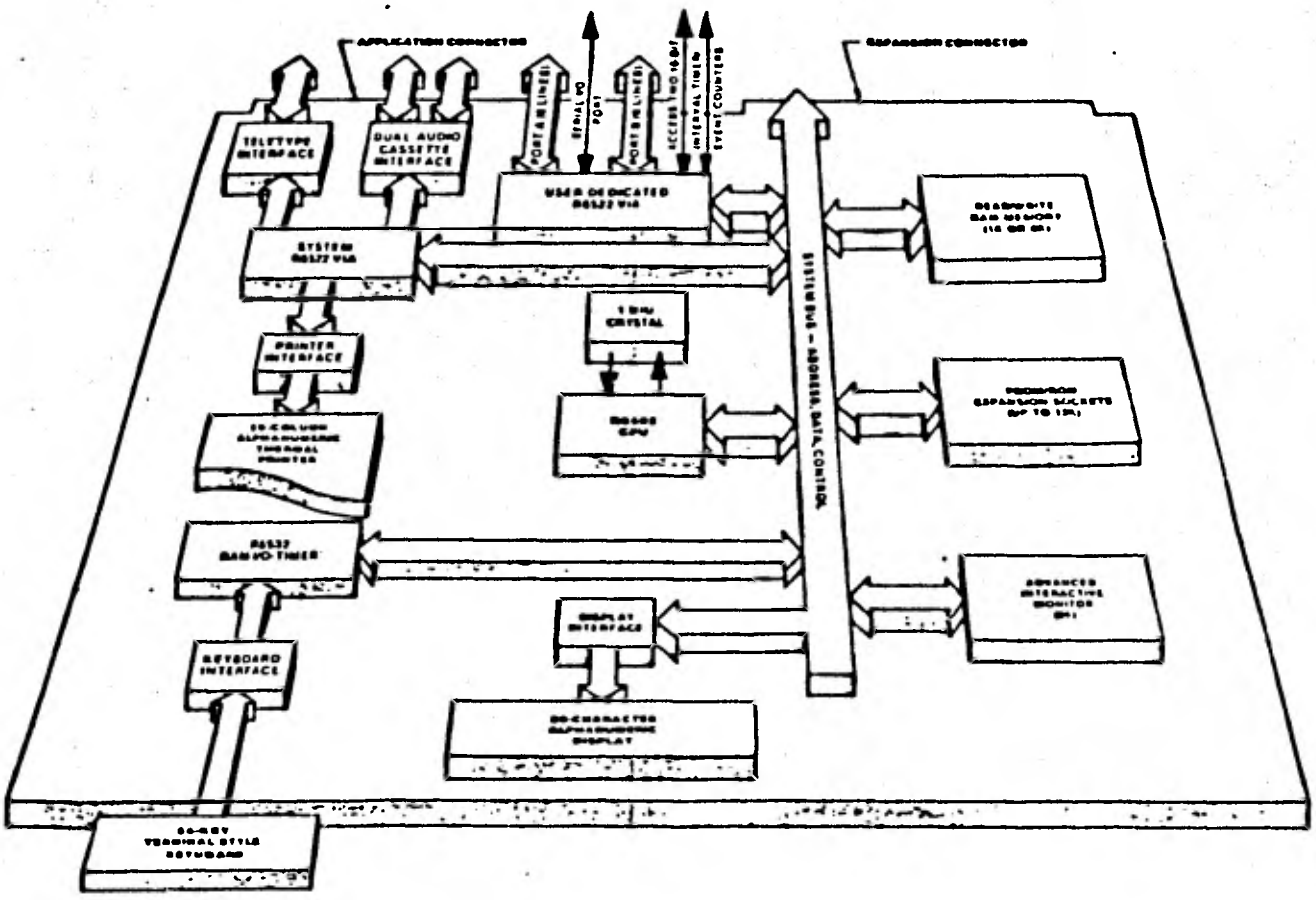


Fig. 17 Diagrama de bloques del AIM-65

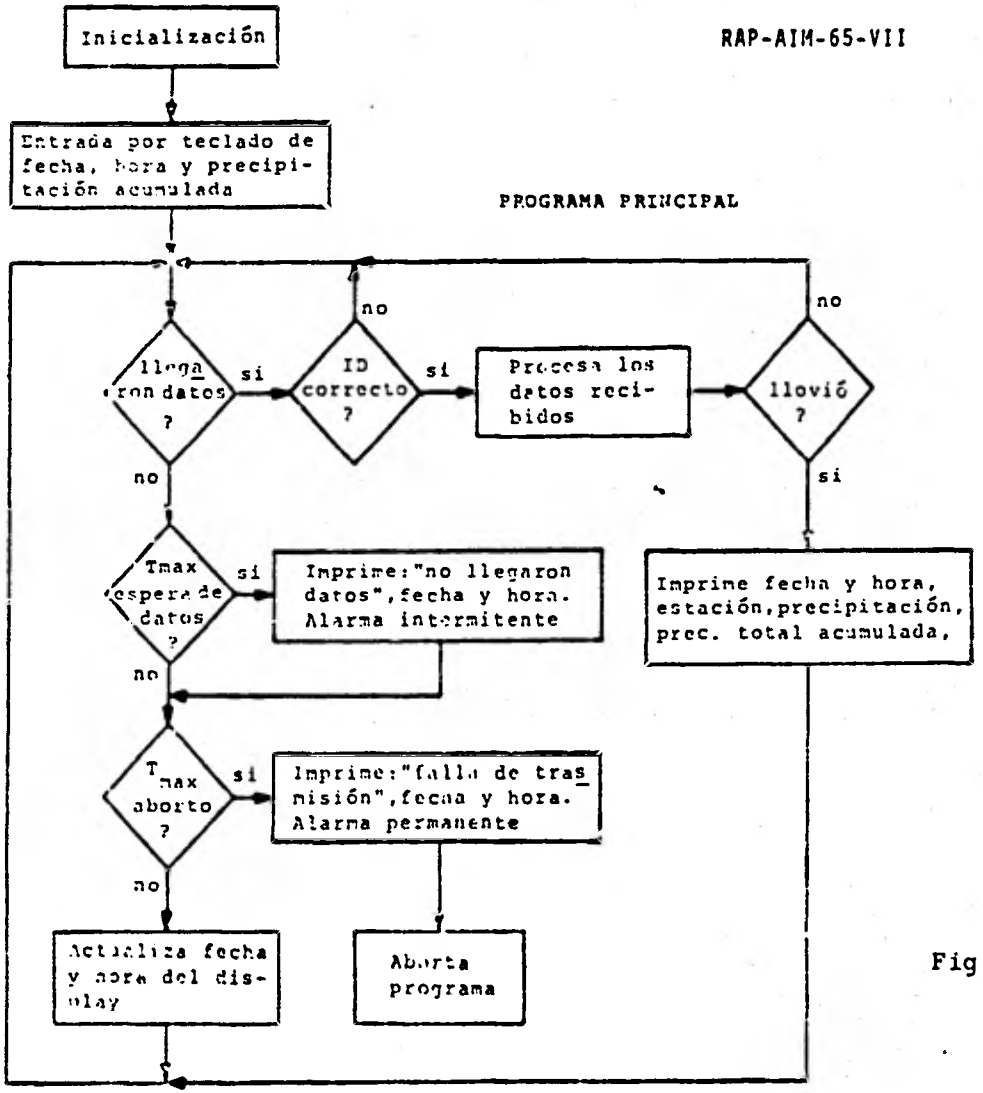
el AIM65 se muestra en la fig. 18.

La ejecución comienza al oprimir la tecla F1, qie inicia el programa con una rutina de inicio; se establecen los parámetros y valores iniciales, se define el direccionamiento de los puertos de entrada/salida y las funciones de interrupción. Por interrogación a través del display, el operador mete por el teclado la fecha (mes, dia, año), hora (hr., min., seg.) y la precipitación total acumulada con la que se desea iniciar. A partir de ese momento se habilitan las interrupciones y da comienzo el programa principal. La primera interrupción se efectúa cuando el UART ha recibido un dato, su rutina de servicio es prioritaria. Una segunda interrupción se da cada segundo y la rutina que da servicio a esta interrupción actualiza el reloj fechador de tiempo real. El segundo se genera decrementando a razón de 1 MHZ un contador cargado inicialmente con el dato F4ØØ HEX (62464 DEC). Repitiendo 16 veces este proceso se obtiene:

$$62464 \text{ M seg} \times 16 = 999.456 \text{ m seg} \approx 1 \text{ seg}$$

En el caso de recibir datos, se analiza el primero, que representa el identificador de estación (ID). Si es incorrecto, el dato fue afectado por ruido o interferencia durante la transmisión radiofónica y se deshecha. Solo cuando ID sea correcto se toman los datos subsiguientes y se procede a su procesamiento. En esta parte del programa se comparan los datos presentes con los datos redundantes de pasadas transmisiones (P_{-1}, P_{-2}, P_{-3}), pudiendo así corregir algún dato incorrecto o no recibido.

Si el resultado del procesamiento de los datos recibidos fue que llovió, se pasa a una rutina en la que se imprime en papel la fecha y hora de arribo de datos, la estación



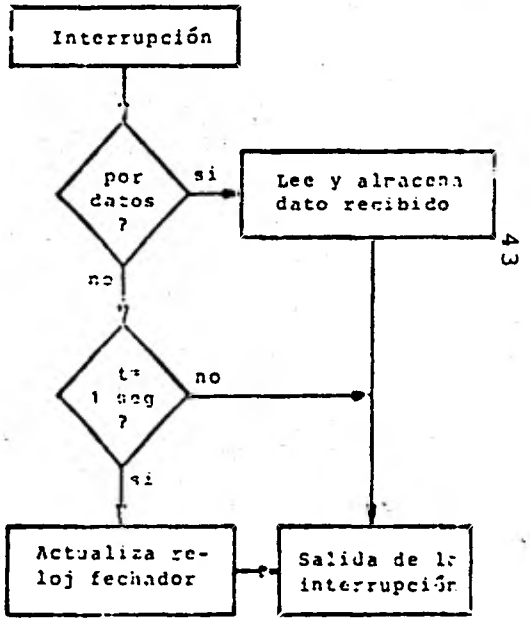


Fig. 18 Ciclo de trabajo en la estación de registro

que los envió, la precipitación y la precipitación total acumulada desde el inicio de la operación.

Mientras no llegan datos, se lleva la cuenta del tiempo transcurrido desde la última recepción por comparación con el reloj propio de tiempo real. Si este es mayor al período programado de transmisión (10 min. típico), se entra a una rutina que imprime el mensaje "NO LLEGARON DATOS" junto con la fecha y hora, y se habilita una alarma audiovisual intermitente. Si el tiempo transcurrido, además es mayor que un límite máximo admisible, el programa imprime el mensaje "FALLA DE TRANSMISION" junto con la fecha y hora, se habilita la alarma en forma permanente y se aborta el programa.

Si la adquisición de datos esta en tiempo, se actualiza la fecha y hora mostrada en el visualizador alfanumérico.

4.4 LISTADO PROGRAMA RAP-AIM-65-VIII

En el apéndice B se presenta el listado del programa RAP-AIM-65-VIII (Registro Automático de precipitación) que se desarrolló para recibir y procesar la información proveniente de la estación de campo (cap. 2 y cap. 3).

4.5 CIRCUITOS ELECTRONICOS

El diagrama general se nuestra en la fig. 19.

4.5.1 DEMODULADOR FSK

La señal de la estación de campo, detectada por el radio receptor, se demodula con el circuito integrado XR2211. Su diagrama de bloques y alambrado se da en la fig. 20. Consiste de un PLL (Phase Locked Loop) para detectar la señal

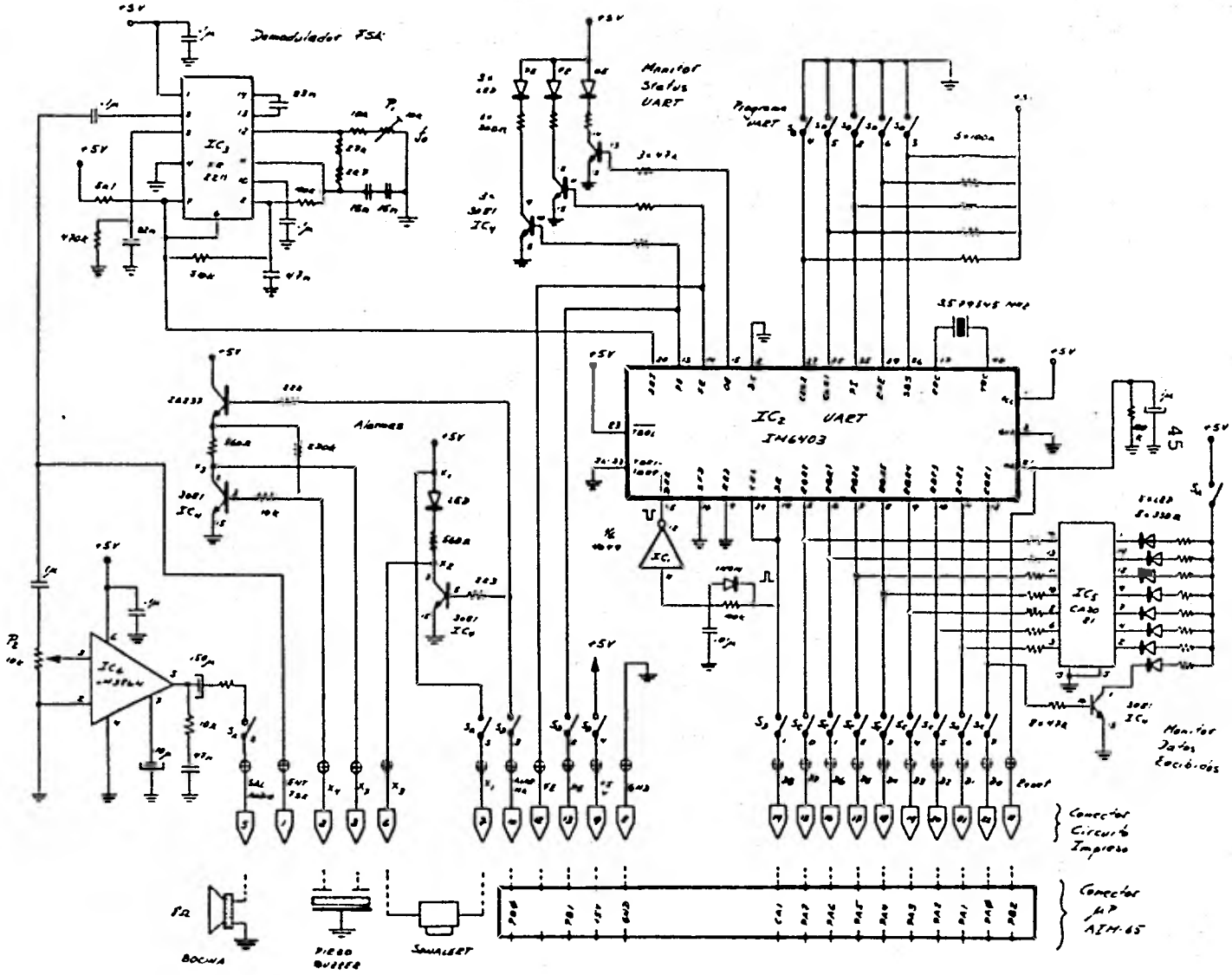


Fig. 19 MODULO RECEPTOR DE DATOS

DIAGRAMA ELECTRONICO

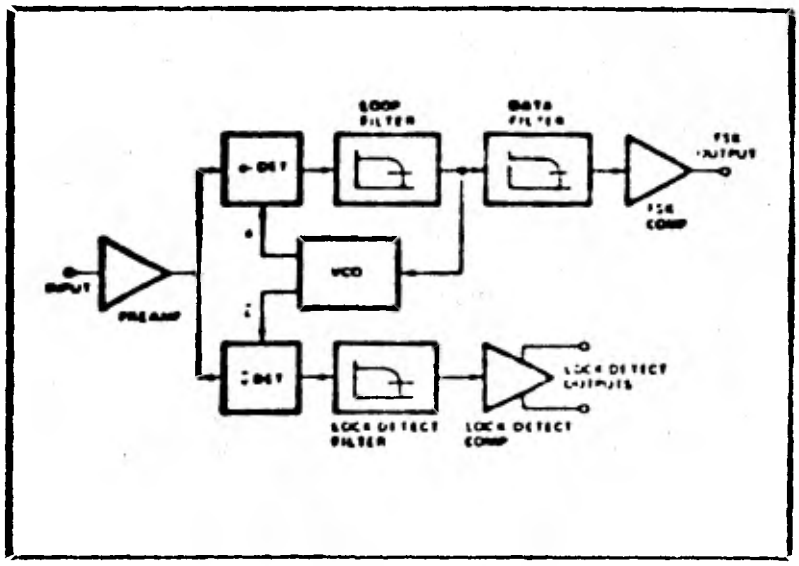


Diagrama de bloques funcional del demodulador FSK XR 2211

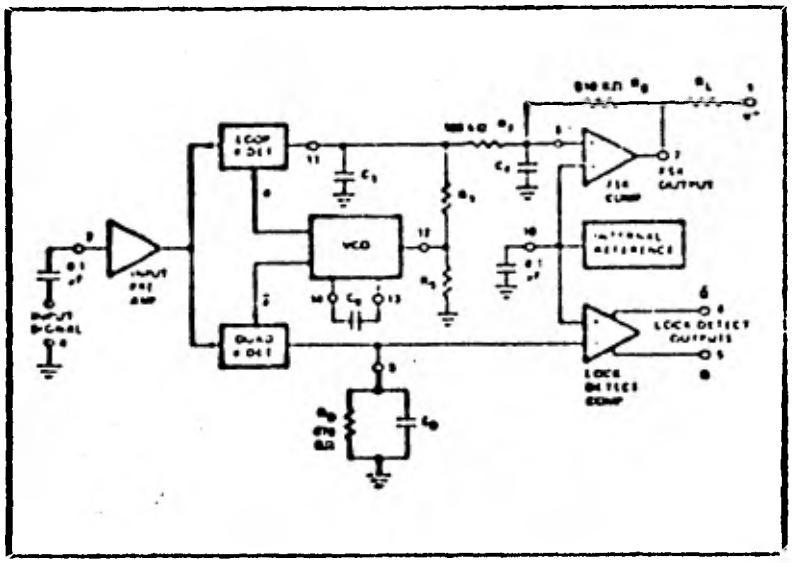


Fig. 20

Diagrama de alambrado del demodulador FSK XR 2211 CP

de entrada en la banda de paso, un detector de fase de cuadratura para detección de portadora y un comparador de voltaje para demodulación FSK. Su diagrama electrónico se muestra en la fig. 19.

Las frecuencias para los niveles lógicos son:

f_1 = 1200 HZ (nivel "0")

f_2 = 2400 HZ (nivel "1")

baud rate = 110

que son las mismas que se usan en la estación de campo al programar el modulador FSK.

4.5.2 UART

El tren de pulsos, con la información seriada detectada en el demodulador FSK, pasa al receptor del UART para ser decodificado y convertido a paralelo. Su circuito se muestra en la fig. 19.

La recepción de datos comienza cuando la entrada RRI cambia de un nivel lógico "1" a "0", transición que indica la llegada de un BIT de inicio. Este bit de inicio será válido, si después de la transición "1" a "0" la entrada RRI permanece en "0" transcurridos 8 pulsos de reloj que es cuando se muestrea. Si la línea está en "1" en el momento del muestreo, el proceso de verificación del BIT de inicio se iniciará de nuevo.

Después de recibido un BIT de inicio válido, de comienzo la recepción de los bits de datos, de paridad y de fin de datos BIT de finalización, de acuerdo a los bits de control escogidos.

Cuando se ha recibido un carácter completo, se transfiere a un registro de salida (RBR1-RBR8) y la señal DR se pone en "1". Esta señal indica al microprocesador que el UART ha recibido un nuevo dato.

DR a su vez se pasa a un circuito monoestable para generar un pulso en la entrada DDR, que pone a cero DR y habilita la recepción de un nuevo dato. (Modo incondicional).

El indicador de control visualiza con LEDS si hubo error de paridad (PE), si no hubo BIT de finalización válida (FE) y si no se puso a cero la línea DR y leído el dato antes de llegar un nuevo carácter (DE). Con el botón RESET se pone a cero PE, FE, OE, DR y es necesario activarlo al prender el circuito.

Al igual que el UART en la estación de campo, la base de tiempo y la velocidad de recepción de 110 bauds, se generan internamente a partir del oscilador a cristal de 3.579545 M Hz.

4.5.3 MONITOR DE AUDIO Y ALARMA

Ya que la señal FSK está dentro de la banda de audio, es posible monitorearla auditivamente. En la fig. 19 se observa el monitor de audio (LM380) que amplifica la señal del receptor y permite verificar su calidad.

Cuando existen problemas en la transmisión, es necesario indicarle al operador la presencia de tal problema. Para ello se instaló una alarma (Sonalert), que es activada cada vez que no llegan datos de la estación de campo o se presenta una falla de transmisión.

A excepción del monitor de audio, que requiere +12VDC, los circuitos operan en +5VDC. Ambos voltajes se derivan de-las fuentes del microcomputador.

4.6 REGISTROS EN PAPEL

Un ejemplo de los registros obtenidos con el enlace-telemétrico descrito, se muestra en la fig. 21.

```
FECHA? MZO 11 90                    ___ Inicialización del
HORA? 08:09:10                          programa
PREC.TOT.ACUM.10000
**********************
**********************
MZO 11 90    08:09:01
EST. II      PREC.  08              ___ Recepción de datos
PREC.TOT.ACUM.   0008
**********************
MZO 11 90    08:11:31
EST. II      PREC.  11
PREC.TOT.ACUM.   0019
**********************
MZO 11 90    08:13:51
EST. II      PREC.  05
PREC.TOT.ACUM.   0024
**********************
MZO 11 90    08:17.57
EST. II      PREC.  07
PREC.TOT ACUM.   0031
**********************
NO LLEGARON DATOS:                  ___ Interrupción de una
MZO 11 90    08:19:16                   trasmisión
**********************
MZO 11 90    08:40:01
EST. II      PREC.  02              ___ Recepción de datos
PREC.TOT.ACUM.   0033
**********************
NO LLEGARON DATOS:                  ___ Interrupción de una
MZO 11 90    08:41:14                   trasmisión
**********************
FALLA DE TRANSMISION:               ___ Interrupción perma-
MZO 11 90    08:45:25                   nente de recepción
**********************                  de datos. Aborto
**********************
```

Fig. 21 Ejemplo de registro de datos

4.7 ESPECIFICACIONES TECNICAS DE LA ESTACION DE REGISTRO

Función:	Recepción, decodificación y registro de datos hidrológicos, enviados desde una estación de campo.
Realización:	Microcomputador AIM65, 8 bits para control de recepción y registro de datos por programa.
Modo de Operación:	Contínuo, recepción asincrona.
Registro:	Impresora sobre papel térmico.
Formato de Impresión:	Fecha y hora de recepción de datos, identificador de estación y precipitación acumulada, precitación total acumulada (ver 4.6-fig. 21).
Codificación de datos:	Paquete de cinco datos: identificador de estación, precipitación acumulada y tres precipitaciones acumuladas anteriores. Formato-tipo ASR-33, 110 bauds: start bit, 5-8 data bits, parity bit, 1-2 stop bits.
Modulación:	FSK. nivel alto ("1") 2400Hz, nivel bajo ("0") 1200 Hz.
Receptor:	Radio "Repco", VHF, 166.69008 MHz, FM calidad voz. Antena Yagi VHF, 5 elementos.

Electrónica:	Digital, MOS, CMOS, Tarjeta circuito impreso.
Suministro de energía eléctrica:	AIM65 y circuitos de recepción:- +24 VDC 2.5 A, +5VDC 2.5 A, - + 12 VDC 500 mA.

5. PERSPECTIVAS DE DESARROLLO

En este capítulo se describe un sistema tentativo para la realización de una estación de campo que sea capaz de llevar a cabo un número mayor de funciones. Es decir, en un sistema de adquisición de datos hidrológicos se requiere conocer una buena cantidad de variables, como pudieran ser: Tirante del río (si es que la estación se encuentra cerca de alguno), temperatura, presión, humedad, voltaje de batería (puésésta es la fuente de energía que hace posible el funcionamiento del equipo), entre otros. En la fig. 22 se observa un diagrama de bloques de lo que sería este sistema. Además se agregó un radio receptor, para el caso general de emplear laestación como retransmisora.

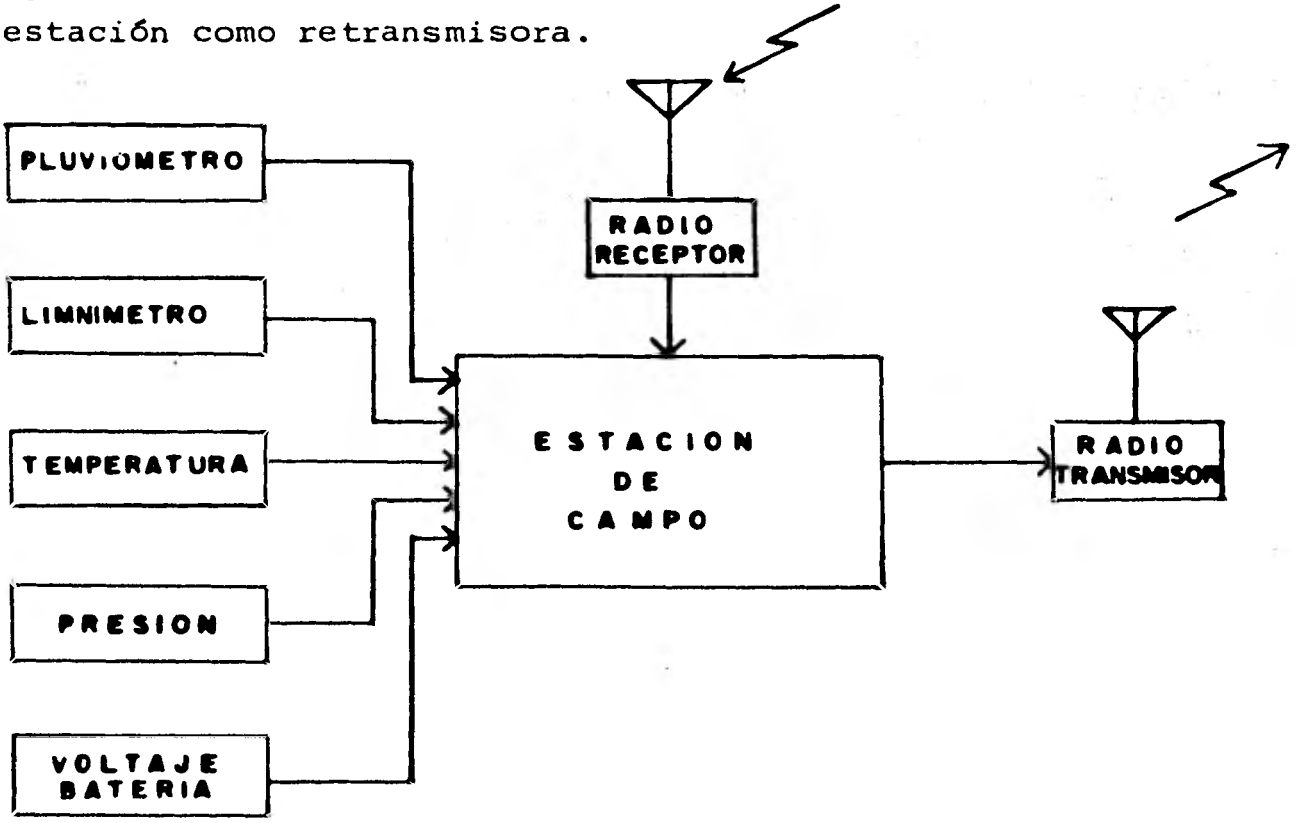


Fig. 22 Diagrama de bloques de la estación de campo

El problema se define como sigue:

Primero: La variable a medirse debe estar dado como un dato binario de ocho bits.

Segundo: Es necesario poner el dato de la variable a medir sobre el bus de datos del microprocesador.

Tercero: Los datos deberán estar presentes, uno a la vez, sobre el bus de datos cada vez que el microprocesador lo requiera.

La solución propuesta a nivel de diagrama de bloques de muestra en la fig. 23.

El primer punto pudiese solucionarse de la siguiente manera: Existe en el mercado un conversor analógico-digital en un circuito integrado monolítico (ADC 0809, ver especificaciones técnicas en el Apéndice A). Este conversor es de ocho canales analógicos y salida de ocho bits en paralelo. Para seleccionar cada canal analógico se conectan los cuatro bits menos significativos del bus de direcciones al decodificador de direcciones del mismo circuito integrado. Este circuito integrado tiene salida con control de alta impedencia (tri-state).

En lo que se refiere al receptor, la señal que llega será en serie. Esta señal se demodula y se hace pasar a un UART que convierte la señal a paralelo. Este circuito también tiene salida de alta impedancia.

Tanto en el receptor como en el pluviómetro, la llegada de un dato o evento es aleatoria. Entonces, para que esos datos no se pierdan deben ser guardados inmediatamente

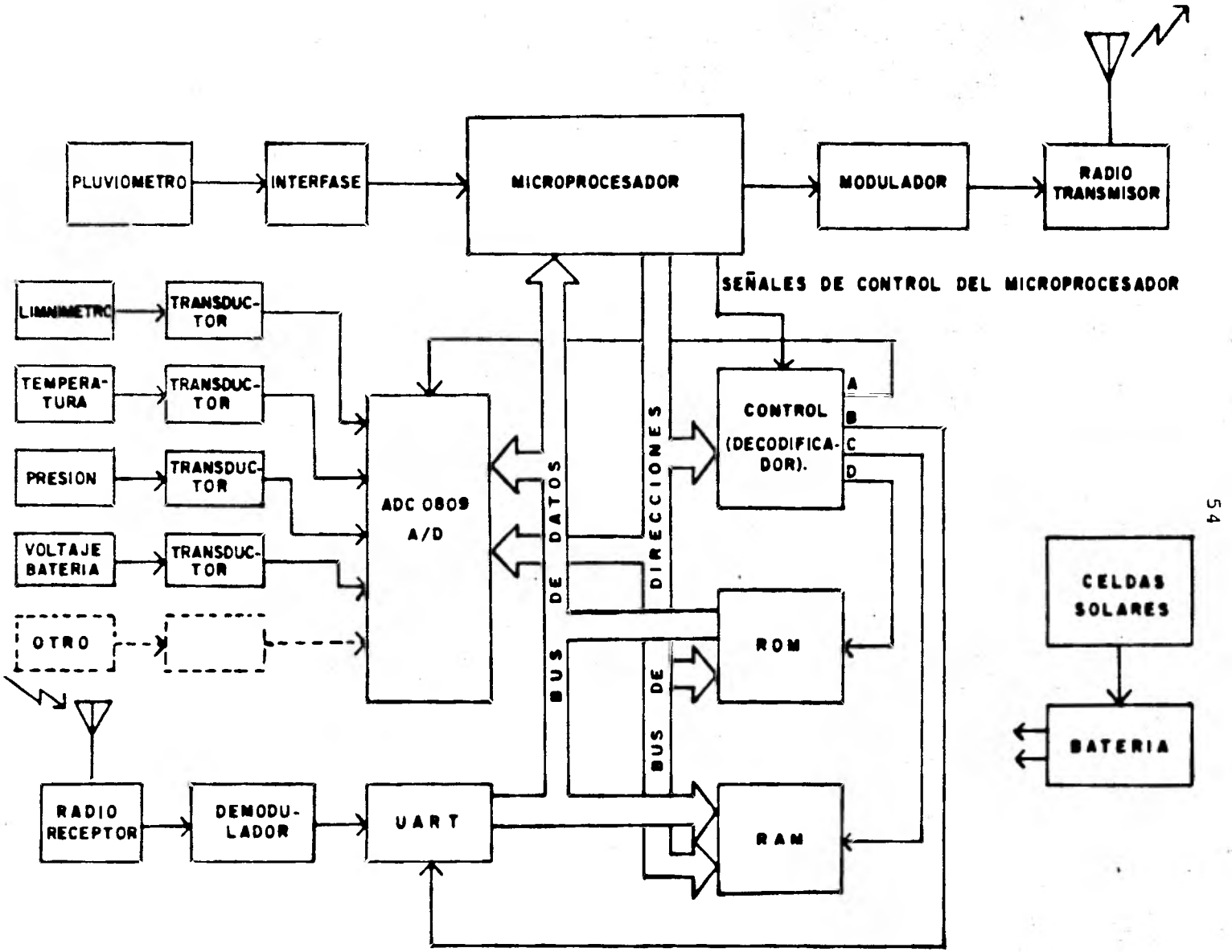


Fig. 23 Perspectiva de la estación de campo

en memoria. Para ello se utilizaría la capacidad de interrupción del microprocesador. Del pluviómetro se mencionó en capitulos pasados como interrumpe al microprocesador; para el caso del UART, este manda un pulso (DR) cada vez que recibe un dato, y es esta señal la que interrumpe la programa en operación, para que el microprocesador de servicio al receptor.

En la fig. 23 se muestran dos memorias (ROM y RAM) conectadas al bus de datos. Ambas memorias tiene salida de alta impedancia. La memoria ROM contendría al programa que controla todas las actividades de esta estación.

El bus de datos consiste en ocho líneas paralelas que llevan o traen información (datos de ocho bits) de un dispositivo periférico o memoria a la unidad central de procesamiento (CPU). Por eso, como el bus de datos está compartido con esos dispositivos, no puede haber más de un dato sobre el bus en un momento dado.

Como se hizo notar, los dispositivos tienen salida de alta impedendancia (tri-state) esto conduce a una plausible solución del tercer punto. Pués para poner un solo dato a la vez sobre el bus sólo hay que accionar uno de los controles de las altas impedancias de los dispositivos. Para ello se tiene en la fig. 23 un bloque denominada CONTROL (Decodificador), cuya función es la de activar sólo una de las salidas de los dispositivos.

El circuito que logra este trabajo se muestra en la fig. 24.

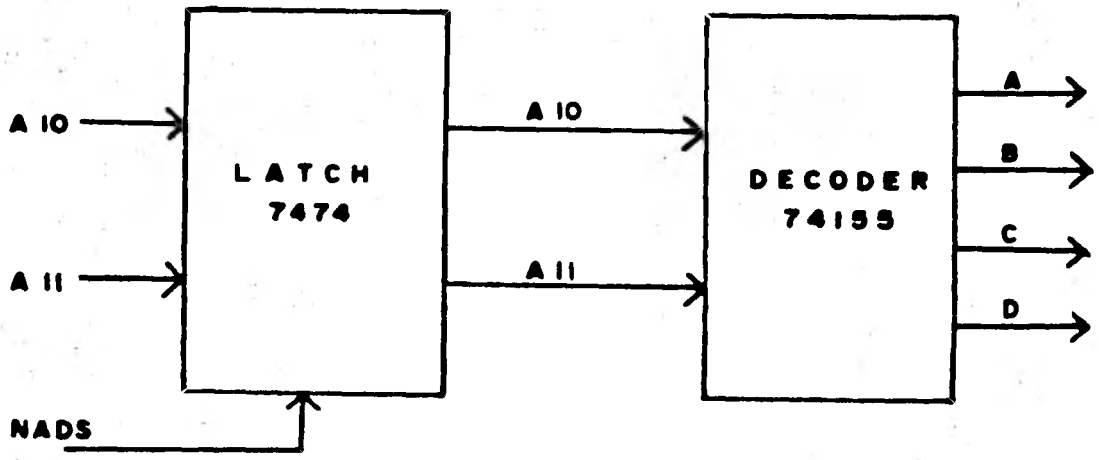


Fig. 24 Circuito decodificador

Consiste de dos circuitos, el primero es un latch - (7474) y el otro un decodificador (74155) de dos entradas - binarias (A10, A11) a cuatro salidas decimales (A, B, C, y D)

Se toman como entrada binarias los dos bits más significativos del bus de direcciones (A10 y A11). Esto significa que en el momento de hacer un direccionamiento los dos -

bits más significativos del bus de direcciones definirán a - que dispositivo se está direccionando.

Con todo lo expuesto anteriormente quedan solucionados los tres puntos que definían al problema. Ahora, la modificación que necesitaría el programa (sub-capitulo 3.2) - sería la de agregar una rutina de servicio para la interrupción del receptor y aumentar el stack de información con los- datos del UART y con los ocho datos del conversor analógico-digital.

6. CONCLUSIONES

Los circuitos y programas descritos en los capítulos anteriores se probaron en condiciones reales de operación. - Y se observaron ventajas y desventajas de unos con respecto - a otros.

La experiencia que se obtuvo al observar el funcio-- namiento de la estación experimental hecha con lógica alambrada fué que es de gran confiabilidad, pués en la temporada de- lluvias de 1979 se logró captar toda la cantidad de precipitación pluvial que se dió en la zona en que se instaló esta - estación.

También cabe recalcar el bajo consumo de corriente - de esta circuitería (trece circuitos integrados y elementos - discretos, incluyendo el transmisor) hecha en base a circui-- tos integrados CMOS que es de aproximadamente 21.7 mA con - un voltaje de alimentación de +12 VDC.

Respecto a la estación de campo hecha con un micro-- procesador, hubo algunos inconvenientes, entre ellos, la alimentación del microprocesador que es de +5VDC y -12 VDC y en- la estación solo se cuenta con alimentación de +12 VDC proveniente de una batería automotríz. Otro problema que se suscitó es el alto consumo de corriente del microprocesador (550 - mA) y por último el circuito es muy sensible a transitorios- en la línea de alimentación.

Pero en general se obtuvieron resultados positivos - en el análisis de este sistema hecho a base de microprocesadores.

Antes que nada la experiencia que se obtuvo en la - adquisición de datos hidrológicos y en el control de procesos de medición remota fué de gran valor. El empleo de microprocesadores facilita el manejo de datos así como la realización de funciones complejas de manera eficiente y confiable.

Además gracias al software se tiene una gran flexibilidad en el diseño, esto es, con instrucciones del procesador se puede resolver problemas de hardware, eliminándose este último en algunos casos. De allí que la electrónica asociada - al microprocesador es muy sencilla.

Por otro lado, comparando costos entre lógica alambrada y microprocesadores, el empleo de un microprocesador - baja el costo del diseño ya que en lógica alambrada se requiere de muchos circuitos integrados, si bien el costo de un circuito integrado es inferior al de un microprocesador, el costo global de todos lo circuitos integrados necesarios para - realizar la lógica alambrada excede en buena cantidad al costo del sistema hecho a base de un microprocesador.

Otro detalle que cabe mencionar es que la operación- intermitente del transmisor permite un ahorro considerable de energía.

Todo este camino recorrido en el campo de los microprocesadores y la tecnología CMOS lleva a que en el futuro - se podrán diseñar nuevos sistemas de adquisición de datos, - los cuales serán mejores y más complejos que los actuales. - Todo ello apoyándose en la creciente tecnología de los microprocesadores.

Otro objetivo al que apunta este camino es el de la disminución del consumo de energía por estos sistemas y esto se logrará empleando en mayor medida circuitos integrados, memorias y microprocesadores CMOS.

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APENDICE A

- Hojas de especificaciones técnicas

  + ISP-5A/500D
  + IM6403IPL
  + TRANSMISOR-RECEPTOR REPCO
  + XR2206
  + XR2211
  + MM5204Q
  + ADC0809

NATIONAL

PRELIMINARY DATA, APRIL 1976

ISP-8A/500D single-chip 8-bit microprocessor (SC/MP)

general description

SC/MP (Simple Cost effective MicroProcessor) is a single chip 8 bit microprocessor packaged in a standard 40 pin dual in line package.

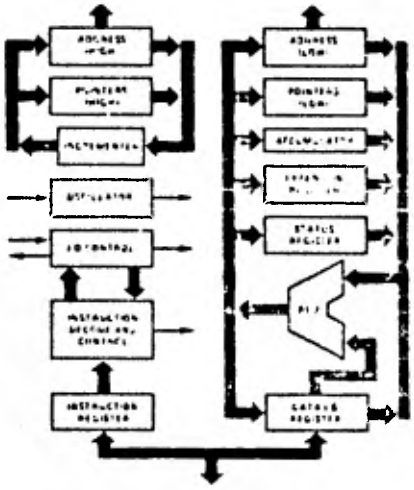
Silicon gate, depletion mode standard process technology ensures high performance, high reliability, and high productability.

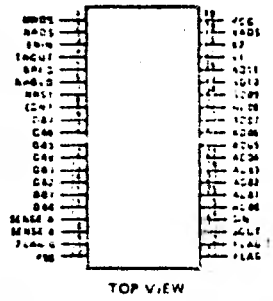
SC/MP is intended for use in general purpose applications where cost per function is a most significant criterion. But cost efficiency is only a part of SC/MP's story. It goes on to include a variety of useful functions that are not even provided by some of the expensive microprocessors, like self contained timing circuitry, 16 bit (65k) addressing capability, serial or parallel data transfer capability and common memory/peripheral instructions. The built in features in conjunction with the low initial cost describe what SC/MP really is — a microprocessor specifically designed to provide the simplest and most efficient solution to many application requirements.

features

- Simpler interfacing
  - Bidirectional TRI STATE® 8 bit data bus
  - TTL compatible input output interface
- Direct Memory Access (DMA) and multiprocessor capabilities
  - Handshake bus access control
- Simplified programming
  - Multiple addressing modes – program counter-relative, immediate data, indexed, auto indexed, and implied
- Direct control output
  - Three user accessible control/flag outputs
- Simpler I/O hardware
  - Separate serial data input and output ports
  - Two sense inputs
  - Direct interfacing to standard memory parts
- On chip timing
  - Minimizes external hardware required for clock generation
- Interface flexibility
  - Capability to interface with memories or peripherals of any speed
- Large system capability
  - Address capability to 65k bytes of memory
- Simplified power requirements

block and connection diagrams





TOP VIEW

Printed in U.S.A.

applications

- Test Systems and Instrumentation
- Machine Tool Control
- Small Business Machines
- Word Processing Systems
- Educational Systems
- Multiprocessor Systems
- Process Controllers
- Terminals
- Traffic Controls
- Laboratory Controllers
- Sophisticated Games
- Automotive

absolute maximum ratings

Voltage at any pin	V_{SS} + 0.3V to V_{SS} - 20V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (T_A = 25°C, V_{SS} = +5V ± 5%, V_{GG} = -7V ± 5%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SPECIFICATIONS					
BANK SHOLD, NRST, SENSE A, SENSE B, SIN, DB0-DB7 (TTL Compatible) (Note 2)					
Logic "1" Input Voltage		V_{SS} - 1		V_{SS} + 0.3	V
Logic "0" Input Voltage	V_{SS} = 5V	V_{SS} - 10	0.8		V
Pull-up Transistor ON Resistance (Note 2)	V_{IN} = (V_{SS} +1)V		7.5		kΩ
Logic "0" Input Current	V_{IN} = 0V		-1.6		mA
BREQ (Note 3)					
Logic "1" Input Voltage		V_{SS} - 1		V_{SS} + 0.3	V
Logic "0" Input Voltage	V_{SS} = 5V		0.8		V
X1, X2 (Note 4)					
Logic "1" Input Voltage		V_{SS} - 1		V_{SS} + 0.3	V
Logic "0" Input Voltage			0.4		V
Input Capacitance (All pins except V_{GG} and V_{SS})			12		pF
Supply Current					
I_{GG}			100		mA
I_{SS}			85		mA
OUTPUT SPECIFICATIONS					
BREQ (Note 3)					
Logic "1" Output Current	V_{OUT} = (V_{SS} +1)V		-2.5		mA
Logic "0" Output Current	(V_{SS} - 10)V ≤ V_{OUT} ≤ V_{SS}		10		μA
External Load Capacitance			50		pF
All Other Outputs					
Logic "1" Output Voltage	I_{OUT} = -200μA	2.4			V
Logic "0" Output Voltage	I_{OUT} = 1.6 mA		0.4		V
External Load Capacitance			75		pF

electrical characteristics (T_A = 25°C, V_{SS} = +5V ± 5%, V_{GG} = -7V ± 5%) (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING SPECIFICATIONS (Note 5)					
T_a minimum (Note 6)			1000		ns
Address and Input/Output Status (See figure 5)					
T_{D1} (ADS)			$3T_a/2$		ns
T_W (ADS)			$(T_a/2) - 300$		ns
T_S (ADDR)			$(T_a/2) - 250$		ns
T_H (ADDR)			50		ns
T_S (STAT)			$(T_a/2) - 250$		ns
T_H (STAT)			50		ns
Data Input Cycle (See figure 5)					
T_D (RDS)			0		ns
T_W (RDS)			$(3T_a/2) - 300$		ns
T_S (RD) minimum			400		ns
T_H (RD) minimum			50		ns
T_{ACC} (RD)			$2T_a - 500$		ns
Data Output Cycle (See figure 6)					
T_D (WDS)			$T_a - 250$		ns
T_W (WDS)			$T_a - 250$		ns
T_S (WD)			$(T_a/2) - 260$		ns
T_H (WD)			100		ns
Input Output Cycle Extend (See figure 7)					
T_S (HOLD)			500		ns
T_{D1} (HOLD)			200		ns
T_{D2} (HOLD)			200		ns
T_W (HOLD)				∞	ns
Bus Access (See figure 4)					
T_D (ENOUT)			300		ns
T_{D2} (ADS)			T_a		ns

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under electrical characteristics.

Note 2: Pullup transistors provided on chip for TTL compatibility.

Note 3: BREQ is an input/output signal that requires an external resistor to V_{GG} or ground.

Note 4: X1 and X2 are master timing inputs that are normally connected to an external crystal or capacitor to control the frequency of the on-chip oscillator. If use of an external oscillator is desired, refer to figure 3 for interconnection details.

Note 5: All times measured from valid Logic "0" or Logic "1" level.

Note 6: T_a is the time period for one clock cycle of the on-chip or external oscillator. Refer to paragraph titled Timing Control for detailed definition.

functional description

SC MP is a self contained general purpose microprocessor designed for ease of implementation in stand alone, DMA (Direct Memory Access), and multiprocessor applications. Communications between SC MP and external memory/peripheral devices are effected via a 12 bit dedicated address bus and an 8 bit bidirectional data bus. During the address interval of each input/output cycle, SC MP employs both buses to provide a 16 bit address output. The 12 least significant address bits are sent out over the 12 bit address bus and the 4 most significant address bits are sent out over the 8 bit data bus along with 4 status bits. Separate strobe outputs from SC MP (NADS, NWDS, NRDS) indicate when valid address information is present on the two busses, and when valid input/output memory or peripheral data are present on the 8 bit bus. To further extend flexibility of application, serial data input/output ports are also provided so that serial data transfers can be effected under program control. The remaining input/output signals shown in Figure 1 are dedicated to general purpose control and status functions, including initialization, bus management, microprocessor halt, interrupt request, input/output cycle extension, and user specified hardware/software interface functions. A detailed description of each input/output signal is provided in table 1.

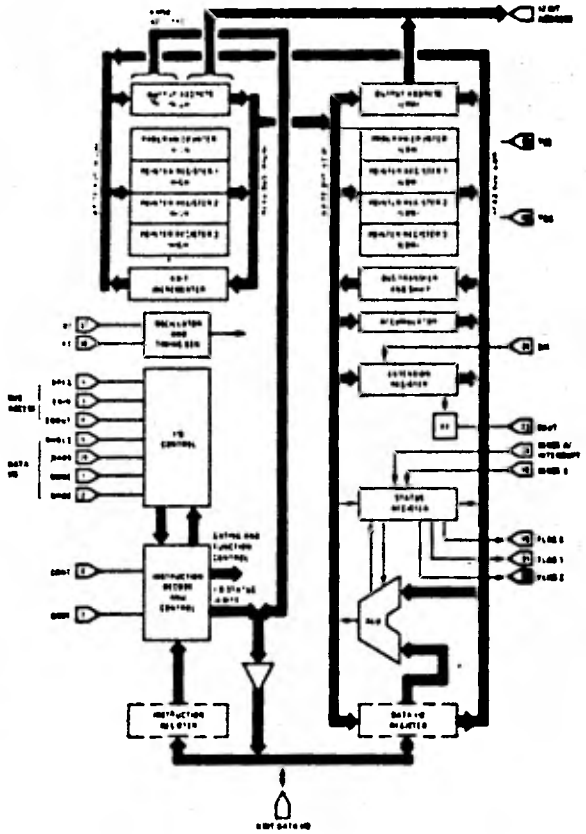


FIGURE 1. SC/MP Division Block Diagram

TABLE 1. Input/Output Signal Description

Signal Mnemonic	Functional Name	Description
NRST	Reset Input	Set high for normal operation. When set low, aborts in process operations. When returned high, internal control circuit zeroes all programmer accessible registers, then, first instruction is fetched from memory location 0001 16
CONT	Continue Input	When set high, enables normal execution of program stored in external memory. When set low, SC/MP operation is suspended after completion of current instruction without loss of internal status.
BREQ	Bus Request Input/Output	Associated with SC MP internal allocation logic for system bus. Can be used as bus request output or bus busy input. Requires external load resistor to V_{GG}
ENIN	Enable Input	Associated with SC MP internal allocation logic for system bus. When set high, SC MP is granted access to system busses. When set low, places system busses in high impedance (TRI STATE®) mode
ENOUT	Enable Output	Associated with SC/MP internal allocation logic for system bus. Set high when ENIN is high and SC/MP is not using system busses (BREQ low). Set low at all other times.
NADS	Address Strobe Output	Active low strobe. While low, indicates that valid address and status output are present on system busses.
NRDS	Read Strobe Output	Active low strobe. On trailing edge, data are input to SC/MP from 8 bit bidirectional data bus. High impedance (TRI STATE®) output when input/output cycle is not in progress.
NWDS	Write Strobe Output	Active low strobe. While low, indicates that valid output data are present on 8 bit bidirectional data bus. High impedance (TRI STATE®) output when input/output cycle not in progress.
NHOLD	Input/Output Cycle Extend Input	When set low prior to trailing edge of NRDS or NWDS strobe, stretches strobe to extend input/output cycle; that is, strobe is held low until NHOLD signal is returned high.
SENSE A	Sense/Interrupt Request Input	Serves as interrupt request input when SC MP internal IE (Interrupt Enable) flag is set. When IE flag is reset, serves as user-designated sense condition input. Sense condition testing is effected by copying status register to accumulator.
SENSE B	Sense Input	User designated sense condition input. Sense condition testing is effected by copying status register to accumulator.
SIN	Serial Input to E Register	Under software control, data on this line are right shifted into E register by execution of SIO instruction.
SOUT	Serial Output from E Register	Under software control, data are right shifted onto this line from E register by execution of SIO instruction. Each data bit remains latched until execution of next SIO instruction.
FLAGS 0, 1, 2	Flag Outputs	User-designated general purpose flag outputs of status register. Under program control, flags can be set and reset by copying accumulator to status register.
AD00 AD11	Address Bit 00 through Address Bit 11	Twelve TRI STATE® address output lines. SC MP outputs 12 least significant address bits on this bus when NADS strobe is low. Address bits are then held valid until trailing edge of read (NRDS) or write (NWDS) strobes. After trailing edge of NRDS or NADS strobe, bus is set to high impedance (TRI STATE®) mode until next NADS strobe.

NOTE:

The 8-bit bidirectional data bus is set to the high-impedance (TRI STATE®) mode except when it is actually in use by SC/MP (NADS, NRDS, or NWDS low). During the addressing interval of each input/output cycle (NADS low), SC/MP provides address and status outputs over the bus; during the ensuing data-transfer interval (NRDS or NWDS low), 8-bit input or output data bytes are routed over the bus.

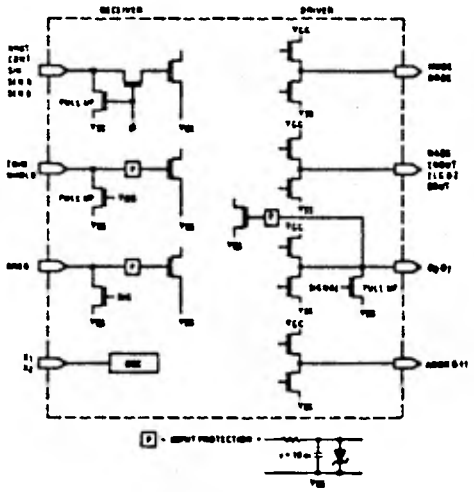
TABLE 1 Input/Output Signal Description (Continued)

Signal Mnemonic/ Pin Designation	Output at NADS Time		Input at NRDS Time	Output at NWDS Time
	Functional Name	Description		
DB0	Address Bit 12	Fourth most significant bit of 16 bit address.	Input data are expected on the eight (DB0-DB7) lines	Output data are valid on the eight (DB0-DB7) lines
DB1	Address Bit 13	Third most significant bit of 16 bit address		
DB2	Address Bit 14	Second most significant bit of 16 bit address		
DB3	Address Bit 15	Most significant bit of 16-bit address.		
DB4	I. Stag	When high, data input cycle is starting; when low, data output cycle is starting		
DB5	I Flag	When high, first byte of instruction is being fetched		
DB6	D Flag	When high, indicates delay cycle is starting, that is, second byte of DLY instruction is being fetched		
DB7	H Flag	When high, indicates that Halt instruction has been executed. (In some system configurations, the H-Flag output is latched and, in conjunction with the CDNTinue input, provides a programmed halt.)	Note: The DB0 through DB7 (AD12 HFLG) lines are a high impedance (open circuit) load when SC/MP does not have access to the input/output bus.	

DRIVERS AND RECEIVERS

Equivalent circuits for SC/MP drivers and receivers are shown below. All inputs have static charge protection circuits consisting of an RC filter and voltage clamp.

These devices still should be handled with care, as the protection circuits can be destroyed by excessive static charge.



SC/MP Driver and Receiver Equivalent Circuits

TIMING CONTROL

All necessary timing signals are provided by an on-chip oscillator and a timing generator. The frequency of the oscillator, in turn, is selected by connecting an external capacitor or crystal between pins 37 and 38 (X1 and X2). When a crystal is used, the resulting frequency of the oscillator is equal to the resonant frequency of the crystal; when a capacitor is used, the frequency of the oscillator varies according to the capacitance value as shown in figure 2.

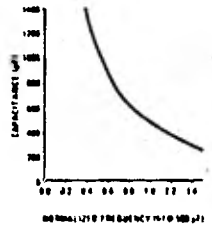


FIGURE 2. Oscillator Frequency versus Capacitance

If desired, the on-chip oscillator can be disabled and the timing generator can be driven by an externally generated clock. In this case, the clock comprises single-phase true and complement inputs. One input is applied to X1 and the other to X2. (A clock is generated at twice the SC/MP clock frequency and is divided by two by a flip-flop as shown in figure 3.)

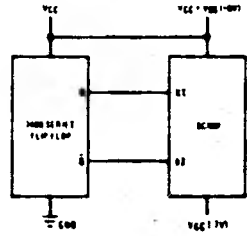


FIGURE 3. External Clock Generation

In the discussions that follow, instruction execution and input/output timing are described in terms of machine cycles. For purposes of definition, the time interval of a machine cycle is computed according to the following formula:

$$1 \text{ machine cycle} = 2T_a$$

where

T_a = time period of oscillator = $\frac{1}{f_{osc}} = \frac{1}{f_{res}} =$ External Clock Frequency

f_{osc} = frequency of on-chip oscillator

f_{res} = resonant frequency of quartz crystal connected between pins 37 and 38

INSTRUCTION FORMAT

The SC/MP instruction repertoire includes both single byte and double byte instructions. A single byte instruction consists of an 8-bit operation code that specifies an operation that SC/MP can execute without further reference to memory. A double byte instruction consists of an 8 bit operation code and an 8 bit data or displacement field. When the second byte represents a data field, the data are processed by SC/MP during execution of the instruction, thereby eliminating the need for further memory references. When the second byte represents a displacement value, it is used to calculate a memory address that will be accessed (written into or read from) during execution of the instruction (refer to Addressing).

DATA STORAGE

As shown in figure 1, SC/MP provides ten internal registers, seven of which are accessible to the programmer. The purpose and function of these registers are described below.

Program Counter — The program counter is a 16 bit register that contains the address of the instruction being executed. The contents of this register are automatically incremented by one just before each instruction is fetched from memory to enable sequential execution of the stored instruction. Under program control, the contents of this register also may be modified or exchanged with the contents of a pointer register to effect subroutine calls and program branches.

NOTE:

The 16 bit address output of the program counter consists of a 4 bit high-order address and a 12 bit low-order address. When the program counter is incremented at the start of each instruction fetch input/output cycle, only the 12 low-order bits are affected; no carry is provided to the 4 high-order bits. For systems employing memories of 4k or less, the high-order bits can be ignored as they are set to 0000_{16} following initialization. For systems employing larger memories, the contents of a pointer register can be modified to select the desired 4k block of memory.

Pointer Registers — The pointer registers are 16 bit general purpose registers that are loaded normally under program control with reference addresses that serve as page pointers, stack pointers, and subroutine pointers. In applications having minimal memory addressing requirements, these registers may be used similarly as data storage registers.

NOTE:

When interrupt requests are enabled, pointer register 3 is automatically referenced by the internal microprogram for formation of the starting address of the user-generated interrupt service routine. (See figure 8.) In this case, the contents of pointer register 3 must be set to one less than the memory location of the first instruction in the interrupt service routine.

Accumulator — The 8 bit accumulator (AC) is the primary working register of SC/MP. It is used for performing and storing the results of arithmetic and logic operations as well as for data transfers, shifts, rotates, and data exchanges with the program counter, the pointer registers, and the status register.

Extension Register – The extension register is used both for serial input/output data transfers and with the accumulator to effect arithmetic, logic, and data transfer operations. If the second byte of an indexed or auto-indexed memory reference instruction (refer to Addressing Modes) equals -128_{10}, the contents of the extension register are used as the displacement value for address formation.

Status Register – The status register provides storage for arithmetic control and software status flags. For more detailed information on the function of this register, refer to Status Register under the description of the Arithmetic and Logic Unit.

Instruction Register – The 8 bit instruction register is not accessible to the programmer. During the fetch phase of each instruction cycle, this register is loaded with the 8 bit instruction operation code retrieved from memory (for a single byte instruction or the first byte of a double byte instruction).

Data Input/Output Register – The data input/output register is not accessible to the programmer. It is used for temporary storage of all input/output data received via or transmitted over the 8 bit bidirectional data bus during the data transfer interval of each input/output cycle (NRDS or NWDS low).

Address Register – The 16 bit address register is not accessible to the programmer. It is used for temporary storage of the 16 bit address transmitted during an input/output cycle.

ARITHMETIC AND LOGIC UNIT

The Arithmetic and Logic Unit (ALU) provides the data manipulation capability that is an essential feature of any microprocessor. The operations provided by the ALU include OR, XOR, increment, decrement, binary addition and decimal addition. For decimal addition, the data inputs to the ALU are treated as two 4 bit BCD digits, thereby eliminating the program storage and execution time required to perform BCD to binary conversion.

BUS TRANSFER LOGIC

The bus transfer logic processes the gating and function control outputs of the instruction decode logic to provide the shift right (with link, without link, or with serial input data), rotate (with or without link), and bus exchange functions necessary for data movement between the SC/MP internal read and write buses. A general summary of the data manipulation capabilities available to the programmer follows:

1. Either the low order or the high order byte of any pointer register can be exchanged with the contents of the 8 bit accumulator. Thus, data exchanges between the pointer registers can be effected one byte at a time via the accumulator.

2. The contents of the program counter can be directly exchanged with the contents of any pointer register.

3. The contents of the extension register can be loaded into the accumulator or can be exchanged with the contents of the accumulator. When the accumulator is loaded from the extension register, the original contents of the accumulator are lost.

4. The contents of the status register can be copied into the accumulator to enable status modification or conditional branch testing. When the status register is copied into the accumulator, the contents of the status register are not altered but the original contents of the accumulator are lost.

5. The contents of the accumulator can be copied into the status register, except for status bits 4 and 5 (Sense A and B inputs to SC/MP). Since these are read only bits, they are not affected by data movements internal to SC/MP. Copying the accumulator into the status register does not alter the contents of the accumulator.

NOTE:

The flag 0, 1, and 2 outputs of the status register serve as latched flags. In other words, they are set to the specified state when the contents of the accumulator are copied into the status register, and they remain in the specified state until the contents of the status register are modified again under program control.

STATUS REGISTER

The function of each bit in the status register is described briefly below:

7	6	5	4	3	2	1	0
CY/L	OV	S_B	S_A	IE	F_2	F_1	F_0

User Flag 0 – User assigned general purpose status bit for implementation as software status bit or in system control applications. This status bit is available as an external output from SC/MP.

User Flag 1 – Same as User Flag 0.

User Flag 2 – Same as User Flag 0.

Interrupt Enable Flag – Internal status bit that is set and reset under program control. When set, SC/MP recognizes external interrupt requests received via Sense A input. When reset, inhibits SC/MP from recognizing interrupt requests.

Sense A – General purpose status input for sensing external conditions. When IE flag is reset, this bit can be tested by copying status register to accumulator. When IE flag is set, this bit serves as interrupt request input causing SC/MP to automatically branch to user generated interrupt service routine in response to high input.

Sense B – Same as Sense A except that it is not tested for interrupt status.

NOTE:

Sense A and B inputs are read only bits. Thus, they are not affected when the contents of the accumulator are copied into the status register.

Overflow (OV) – This bit is set if an arithmetic overflow occurs during an add (ADD, ADI, or ADE) or a complement and add instruction (CAD, CAI, or CAE). It is not affected by the decimal add instructions (DAD, DAI, or DAE).

Carry/Link (CY/L) – This bit is set if a carry from the most significant bit occurs during an add, complement and add, or decimal add instruction. Thus, it serves as a carry input to the next add instruction. In addition, it is included in the Shift Right with Link (SRL) and Rotate Right with Link (RRL) instructions.

CONTROL

The operation of the SC/MP microprocessor consists of repeatedly accessing or fetching instructions from the program stored in external memory and executing the operations specified by the instructions. These two steps are carried out under the control of an internal microprogram. (SC/MP is not user microprogrammable.) The microprogram is similar to a state table specifying the series of states of system control signals necessary to carry out each instruction. Microprogram storage is provided in the instruction decode and control logic, and microprogram routines are implemented to fetch and execute instructions. The fetch routine first increments the program counter, and then carries the instruction address to be transferred from the program counter to the system busses via the output address register. The microprogram next initiates an input data transfer. When the instruction operation code is subsequently placed on the 8 bit data bus (single byte instruction or first byte of double byte instruction), the operation code is loaded into the instruction register. The operation code is then partially decoded to determine whether the instruction contains a second byte. If it does, a second input data transfer is effected to load the next byte in the data input/output register.

After the complete instruction is stored in the instruction and/or data input/output register(s), the instruction decoder transforms the instruction operation code into the address of the appropriate instruction execution routine contained in the internal microprogram. The microprogram then branches to the specified internal address to initiate execution of the instruction. The resulting execution routine comprises one or more microinstructions that implement the required functions. For example, the first microcycle of an Extension Register Add Instruction (ADE) causes the contents of the extension register to be gated onto the read bus, transferred to the write bus via the bus control logic, and then written into the data input/output register. The next microcycle causes the contents of the accumulator to be gated onto the read bus, the contents of the read bus to be added to the contents of the data input/output register via the ALU, and the resultant output of the ALU to be written into the accumulator via the write bus. The final step of the execution routine is a jump back to the fetch routine to access the next instruction.

INITIALIZATION

Since SC/MP may power up in a random condition, the following power up and initialization procedure is recommended:

1. Apply power (V_{SS} and V_{GG}) and set NRST low.

NOTE:

Allow ample time (typically, 100ms) for the oscillator and the internal clocks to stabilize. In systems where NRST is set low after turning on power, NRST must remain low for a minimum of $4T_X$. While NRST is low, any in process operations are aborted automatically. When NRST is low, strobes and address and data busses are in the Non I/O state (high Z state).

2. Set NRST high.

NOTE:

This causes the SC/MP microprocessor to set the contents of all programmer accessible registers to zero. Thus, when SC/MP is granted access to the system busses following initialization, the first instruction is fetched always from memory location 0001₁₆. The BREQ output goes high, indicating the start of this input/output cycle, this occurs at a time within $13T_X$ after NRST is set high. Normal execution of the program continues as long as NRST remains high.

parallel data transfers

Parallel data transfers occur during each instruction fetch and during the ensuing read/write cycle associated with execution of the memory reference instructions. This class of instruction could perhaps more precisely be called the "Input Output Reference Class". In the case of the SC/MP microprocessor, since all data transfers, whether with memory, peripheral devices, or a central processor data bus, occur through the execution of these instructions. This unified bus structure is in contrast with many other microprocessors and minicomputers that have one instruction type (input output class) for communication with peripheral devices and another instruction type (memory reference class) for communication with memories. The advantage of the approach taken by SC/MP is that a wider variety of instructions (the entire memory reference class) is available for communications with peripherals. Thus, the LD and ST (Load and Store) instructions can be used for basic transfers, the ILD and DLD (increment/decrement and load) instructions can be used for indexing peripheral registers, and the remaining memory reference instructions can be used, as required, for "one step" retrieval and processing of peripheral input data.

BUS ACCESS

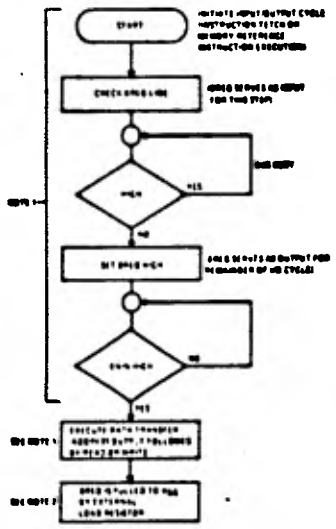
Before SC/MP can initiate parallel I/O transfers with memory or peripheral devices, it must have access to the system address and data busses. Three of the SC/MP input/output signals are associated with bus control: BREQ, ENIN, and ENOUT. For simple stand-alone applications, the ENOUT signal can be ignored and the ENIN signal can be tied to V_{SS} to allow the SC/MP microprocessor to have continual access to the system busses. The BREQ input/output line then goes high during each input/output cycle as shown in figures 5 and 6 to indicate when SC/MP is actually using the system busses.

NOTE:

The BREQ input/output line must be tied to V_{GG} (or ground in +5 volt/-12 volt systems) via an external load resistor to allow normal operation of the SC/MP microprocessor.

For DMA and multiprocessor applications, the BREQ, ENIN, and ENOUT signals can be interconnected in various configurations to allow bus access to be granted to requesting devices according to user specified priorities. Figure 4 illustrates the general sequence in which these signals are processed by SC/MP to gain access to the system busses and to indicate when the busses are actually being used.

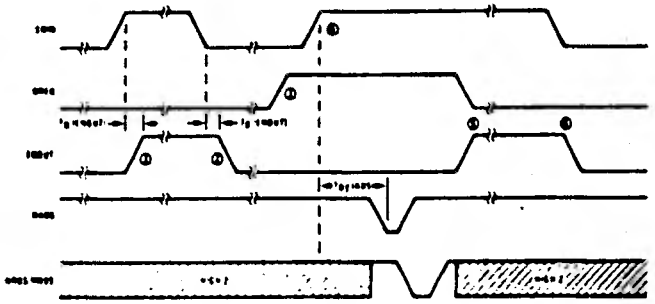
A. BREQ AND ENIN PROCESSING SEQUENCE



Note 1: ENOUT is always low while SC/MP is actually using bus, that is, ENIN input and BREQ output are high.

Note 2: When SC/MP is not using bus (BREQ output or ENIN input low), ENOUT is held in same state as ENIN input.

B. BREQ, ENIN, and ENOUT Timing



Note 1: ENOUT goes high to indicate that SC/MP was granted access to bus (ENIN high) but is not using bus.

Note 2: ENOUT goes low in response to low ENIN input.

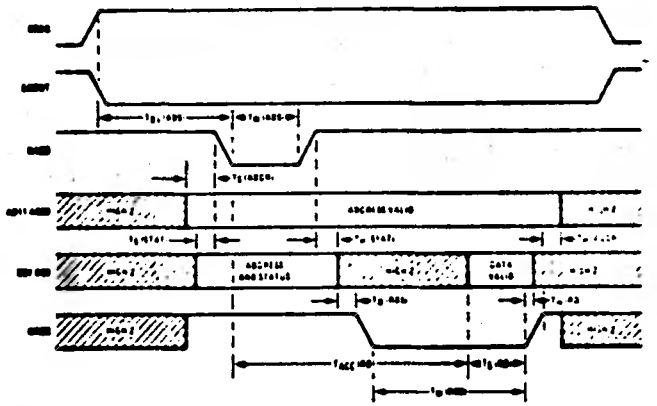
Note 3: SC/MP generates bus request, bus access not granted because ENIN low.

Note 4: ENIN goes high. Bus access now granted and input/output cycle actually initiated. If ENIN is set low while SC/MP has access to the bus, the address and data ports will go to the high impedance (TRI STATE®) state, but BREQ will remain high. When ENIN is subsequently set high, the input/output cycle will begin again.

Note 5: I/O cycle completed. ENOUT goes high to indicate that SC/MP granted access to bus but not using bus. If ENIN had been set low before completion of input/output cycle, ENOUT would have remained low.

Note 6: ENOUT goes low to indicate that system busses are available for use by highest-priority requester.

FIGURE 4. Bus Access Control



Note: Timing is valid when ENIN is wired high or is set high before BREQ is set high by SC/MP; see figure 4 for NADS timing when ENIN is set high after BREQ.

FIGURE 5. SC/MP Bus Input Timing

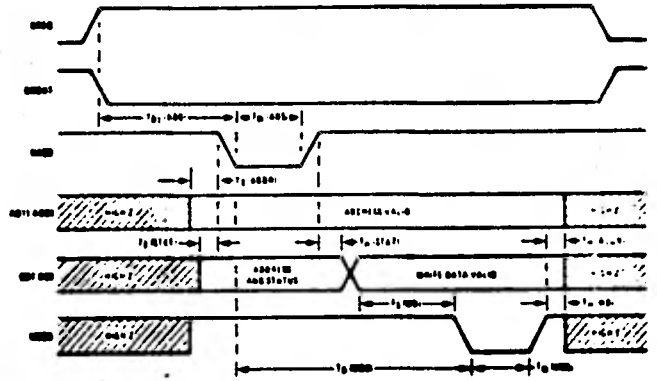


FIGURE 6. SC/MP Bus Output Timing

INPUT/OUTPUT CYCLE

Once SC/MP has control of the system busses, the actual input/output cycle begins. As shown in figures 5 and 6, the functions of memory addressing, data reading, and data writing are implemented, respectively, by the address strobe (NADS), the read strobe (NRDS), and the write strobe (NWDS). Note that the BREQ signal is reset low at the end of the input/output cycle to indicate that the system busses are now free for use by the highest priority requesting device.

The first operation that SC/MP performs for each input/output cycle is to load the 12 least significant address bits onto the 12 bit address bus, and the 4 most significant address bits along with 4 status bits onto the 8 bit data bus. At the same time SC/MP sets the NADS output low to indicate that the address and the status information are valid. The low order address on the 12 bit bus is then held valid for the duration of the input/output cycle, the high order address and the status information on the 8 bit bus remain valid only while NADS is low. While valid, the status bits have the following significance:

MFLG – When high, indicates that input/output cycle is read cycle; when low, indicates that input/output cycle is write cycle.

IFLG – Set high to indicate that instruction operation code (single byte instruction or first byte of double byte instruction) will be output from memory following NADS.

DFLG – Set high only when second byte of Delay instruction is to be read from memory following NADS. Execution of the Delay instruction then starts at trailing edge of NRDS. Upon completion, SC/MP provides NADS output to initiate next input/output cycle if bus access is granted. Time in microcycles from leading edge of delay flag to trailing edge of subsequent NADS output is computed from the following formula:

$$\text{Delay} = 19 + 2(\text{ACC}) + 2\,\text{disp} + 2^9\,\text{disp}\ \text{microcycles}$$

where

(ACC) = unsigned contents of accumulator

disp = unsigned displacement value contained in second byte of Delay instruction

The time derived from the above formula does not include the four microcycles required to fetch the first byte of the Delay instruction. Thus, when the Delay instruction is used for software timing, total instruction execution time equals (13 + 2(ACC) + 2 disp + 2^9 disp) microcycles.

NOTE:

When Halt instruction is executed, instruction decode and control logic inhibits incrementing of program counter for one input/output cycle. Thus, Halt instruction is read from memory a second time to enable generation of HFLG output, but no further processing of Halt instruction occurs. In effect, this procedure ensures HFLG is output in advance of the next instruction to be fetched from memory.

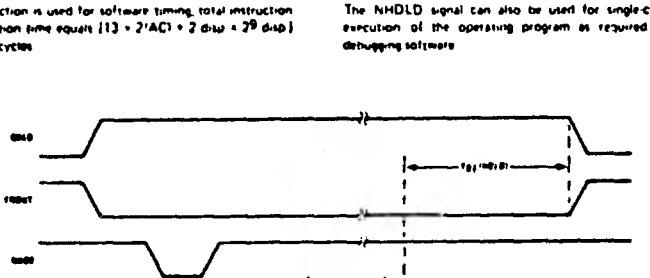
HFLG – Set high only during addressing interval of read cycle that follows Halt instruction. HFLG may be used to cause user-provided external logic to set the CONT input low, and thereby to effect a programmed halt. Since HFLG read cycle precedes the next instruction fetch, termination of programmed halt enables fetch of first instruction that follows Halt instruction.

After resetting the NADS output, SC/MP generates an NRDS or NWDS strobe, respectively, to initiate a data input (read) or data output (write) operation. For a read operation, input data are strobed into SC/MP from the 8 bit bus on the trailing edge of the NRDS strobe. For a write operation, SC/MP places valid output data on the 8 bit bus on the trailing edge of the NWDS strobe. After resetting the NRDS or NWDS strobe to complete the data transfer, SC/MP then resets the BREQ signal to indicate that the system busses are free for use by another controller.

input/output cycle extension

For systems employing memories or peripherals with long access times, it may be desirable to utilize the NHOLD input to lengthen the input/output cycle. As shown in figure 7, setting the NHOLD signal low prior to the trailing edge of the NRDS or NWDS strobe causes SC/MP to hold the strobe active until after the NHOLD signal is returned high.

The NHOLD signal can also be used for single-cycle execution of the operating program as required for debugging software.



Note: Dashed trailing edge of NRDS, NWDS indicates normal strobe timing when NHOLD is not active.

FIGURE 7 – Extended Input/Output Timing

serial data transfers

Serial input/output data transfers can be used efficiently with very slow input/output peripherals such as X-Y plotters, teletypewriters, slow-speed printers, and so forth. Such transfers can be effected in any of the following manners:

1. By assigning serial input/output functions to the extension register via the SIO (Serial Input/Output) instruction. When this instruction is executed, the contents of the extension register are shifted right one bit. At the same time, data present on the SIN line are shifted into bit position 7 of the extension register and the original contents of bit position 0 are shifted into a flip-flop to provide a latched output of the SOUT line. The SOUT data are then held latched until the next SIO instruction is executed.

2. By using one of the status flags at an output data bit and one of the sense lines as an input data bit.

3. By implementing external logic such that only one line of the 8 bit data input/output bus is used.

For synchronous systems, serial data input/output timing may be provided by program loops that employ the delay instruction, or by using one or more of the transfer instructions (see table 2) to test the output of an external timing circuit. For asynchronous systems, one of the sense inputs can be used for testing bit received-ready status and a pulsed flag output can be provided, under program control, for peripheral indexing each time that a data bit is actually shifted in or out.

Systems that have several input/output devices must be multiplexed. Device selection can then be accomplished using the status flag outputs of SC/MP, or by using parallel input/output commands to load an external latch. Systems that do not require serial input/output capability can employ the SIN and SOUT lines as a sense input and flag output, respectively.

interrupts

When the internal interrupt enable (IE) flag is set under program control, the Sense A line is enabled to serve as an interrupt request input. When the IE flag is reset, SC/MP is inhibited from detecting interrupts. Thus, while the IE flag is set, the Sense A input is tested prior to the fetch phase of each instruction as shown in figure 8. Upon detection of an interrupt request (Sense A high), the following events occur automatically:

1. The status register IE flag is reset to prevent SC/MP from responding to any further interrupt requests. Interrupt request capability can then be re-enabled during or at the end of the existing user-generated interrupt service routine via the IEN (Enable Interrupt) instruction by copying the accumulator into the status register.

2. The contents of the program counter are exchanged with the contents of the pointer register 3.

3. The contents of the program counter are incremented by one to address the first instruction of the user-generated interrupt service routine.

The interrupt system must be armed before interrupts are enabled. This is accomplished as follows:

1. First, the Interrupt Enable Bit in the Status Register is set true by executing either an Enable Interrupt instruction (IEN) or a Copy Accumulator to Status Register instruction (CAS).

2. Second, one additional instruction is fetched and executed.

A return from interrupt is accomplished by executing two instructions: Enable Interrupt (IEN) immediately followed by Exchange Pointer 3 with Program Counter (XPPC 3).

microprocessor halt

The CONT input to SC/MP is provided to enable suspension of operation without loss of internal status. Processing of the CONT input is shown in figure 8. Since this is an asynchronous input, it can be controlled by external timing logic, or as stated previously, the HALT flag output that appears on the 8 bit data bus during the read cycle that follows execution of a Halt instruction can be used with an external circuit to effect a programmed halt condition. Note that when an interrupt request is detected with the CONT input is low, the first instruction of the user-generated interrupt service routine is automatically executed. Thus, the first instruction of the interrupt service routine can be used to reset the external CONT input logic and, thereby, to terminate the microprocessor halt condition if so desired.

After execution of an instruction, the CONT input must be high for a minimum time of $2T_R$ (1 microcycle) in order to fetch and execute the next instruction.

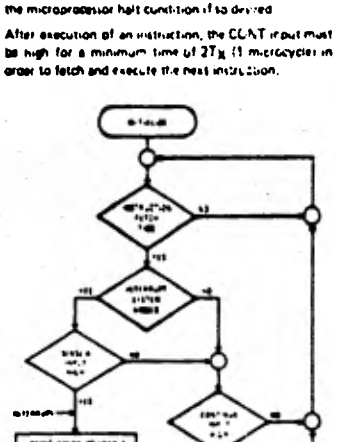


FIGURE 8

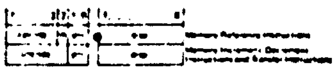
Microprocessor Halt and Interrupt Request Input Processing

instruction set

The SC/MP instruction set provides the general purpose user of microprocessors a powerful programming capability along with above average flexibility and speed. The instruction set consists of 46 instructions, which comprise eight general categories. A listing of the complete instruction set is presented in table 2; typical instruction execution times are given in table 3, and notations and symbols used as shorthand expressions of instruction capabilities are defined in table 4.

ADDRESSING

During execution, instructions and data defined in a program are stored into and loaded from specific memory locations, the accumulator or selected registers. Because SC/MP, memory (read/write and read only), and peripherals are on a common data bus, any instruction used to address memory may be used to address the peripherals. The formats of the instruction groups that reference memory are shown below.



Memory reference instructions use the PC-relative, indexed, or auto-indexed methods of addressing memory. The memory increment/decrement instructions and the transfer instructions use the PC-relative or indexed methods of addressing.

The various methods of addressing memory and peripherals are shown below.

Immediate addressing is an addressing format specific to the immediate instruction group.

Type of Addressing	Operand Formats		
	m	ptr	disp
PC-relative	0	0	-128 to +127
Indexed	0	1, 2, or 3	-128 to +127
Immediate	1	0	-128 to +127
Auto-indexed	1	1, 2, or 3	-128 to +127

For PC-relative, indexed, and auto-indexed memory-reference instructions, another feature of the addressing architecture is that the contents of the extension register are substituted for the displacement if the instruction displacement equals -128 (-X'80).

NOTE:

All arithmetic operations associated with address formation affect only the 12 low-order address bits; no carry is provided to the 4 high-order bits. For systems employing memories of 4k or less, the high-order bits can be ignored as they are set to 0000 following initialization. For systems employing larger memories, the high-order bits must be set to the starting address of the desired 4k block of memory. For example:

0001_2 enables memory locations 1000_{16} - $1FFF_{16}$ to be addressed.

0010_2 enables memory locations 2000_{16} - $2FFF_{16}$ to be addressed and so forth.

PC-Relative Addressing – A PC-relative address is formed by adding the displacement value specified in the operand field of the instruction to the current contents of the program counter. The displacement is an 8-bit twos complement number, so the range of the PC-relative addressing format is -128_{10} to $+127_{10}$ locations from the current contents of the program counter.

Immediate Addressing – Immediate addressing uses the value in the second byte of a double-byte instruction as the operand for the operation to be performed (see below).

For example, compare a Load (LD) instruction to a Load Immediate (LDI) instruction. The Load instruction uses the contents of the second byte of the instruction in computing the effective address of the data to be loaded. The Load Immediate instruction uses the contents of the second byte as the data to be loaded.

Indexed Addressing – Indexed addressing enables the programmer to address any location in memory through the use of the pointer register and the displacement. When indexed addressing is specified in an instruction, the contents of the designated pointer register are added to the displacement to form the effective address. The contents of the pointer register are not modified by indexed addressing.

Auto-Indexed Addressing – Auto-indexed addressing provides the same capabilities as indexed addressing along with the ability to increment or decrement the designated pointer register by the value of the displacement. If the displacement is less than zero, the pointer register is decremented by the displacement before the contents of the effective address are fetched or stored. If the displacement is equal to or greater than zero, the pointer register is used as the effective address, and the pointer register is incremented by the displacement after the contents of the effective address are fetched or stored.

TABLE 2. SC/MP Instruction Summary

DOUBLE BYTE INSTRUCTIONS

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO CYCLES
	Memory Reference Instructions	7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0		
LD	Load	1 1 0 0 0 m ptr / disp	(AC)←(EA)	18
ST	Store	1 1 0 0 1	(EA)←(AC)	18
AND	AND	1 1 0 1 0	(AC)←(AC)∧(EA)	18
OR	OR	1 1 0 1 1	(AC)←(AC)∨(EA)	18
XOR	Exclusive-OR	1 1 1 0 0	(AC)←(AC)⊕(EA)	18
DAD	Decimal Add	1 1 1 0 1	$(AC)\leftarrow(AC)_{10}+(EA)_{10}+(CY/L),(CY/L)$	23
ADD	Add	1 1 1 1 0	(AC)←(AC)+(EA)+(CY/L), (CY/L), (OV)	19
CAD	Complement and Add	1 1 1 1 1	(AC)←(AC)+~(EA)+(CY/L), (CY/L), (OV)	20
	Memory Increment/Decrement Instructions	7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0		
ILD	Increment and Load	1 0 1 0 1 0 ptr / disp	(AC), (EA)←(EA)+1	22
DLD	Decrement and Load	1 0 1 1 1 0	(AC), (EA)←(EA)−1	22
	Immediate Instructions	7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0		
LDI	Load Immediate	1 1 0 0 0 1 0 0 / data	(AC)←data	10
ANI	AND Immediate	1 1 0 1 0 1 0 0	(AC)←(AC)∧data	10
ORI	OR Immediate	1 1 0 1 1 1 0 0	(AC)←(AC)∨data	10
XRI	Exclusive-OR Immediate	1 1 1 0 0 1 0 0	(AC)←(AC)⊕data	10
DAI	Decimal Add Immediate	1 1 1 0 1 1 0 0	$(AC)\leftarrow(AC)_{10}+data_{10}+(CY/L),(CY/L)$	15
ADI	Add Immediate	1 1 1 1 0 1 0 0	(AC)←(AC)+data+(CY/L), (CY/L), (OV)	11
CAI	Complement and Add Immediate	1 1 1 1 1 1 0 0	(AC)←(AC)+~data+(CY/L), (CY/L), (OV)	12
	Transfer Instructions	7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0		
JMP	Jump	1 0 0 1 0 0 ptr / disp	(PC)←EA	11
JP	Jump if Positive	1 0 0 1 0 1	If (AC)≥0, (PC)←EA	9, 11
JZ	Jump if Zero	1 0 0 1 1 0	If (AC)=0, (PC)←EA	9, 11
JNZ	Jump if Not Zero	1 0 0 1 1 1	If (AC)≠0, (PC)←EA	9, 11
	Double Byte Miscellaneous Instructions	7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0		
DLY	Delay	1 0 0 0 1 1 1 1 / disp	count AC to −1, delay = 13 + 2(AC) + 2 disp + 2^9 disp microcycles	13 to 131,593

SINGLE BYTE INSTRUCTIONS

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO CYCLES
	Extension Register Instructions	7 6 5 4 3 2 1 0		
LDE	Load AC from Extension	0 1 0 0 0 0 0 0	(AC)←(E)	6
XAE	Exchange AC and Extension	0 0 0 0 0 0 0 1	(AC)↔(E)	7
ANE	AND Extension	0 1 0 1 0 0 0 0	(AC)←(AC)∧(E)	6
ORE	OR Extension	0 1 0 1 1 0 0 0	(AC)←(AC)∨(E)	6
XRE	Exclusive-OR Extension	0 1 1 0 0 0 0 0	(AC)←(AC)⊕(E)	6
DAE	Decimal Add Extension	0 1 1 0 1 0 0 0	$(AC)\leftarrow(AC)_{10}+(E)_{10}+(CY/L),(CY/L)$	11
ADE	Add Extension	0 1 1 1 0 0 0 0	(AC)←(AC)+(E)+(CY/L), (CY/L), (OV)	7
CAE	Complement and Add Extension	0 1 1 1 1 0 0 0	(AC)←(AC)+~(E)+(CY/L), (CY/L), (OV)	8
	Pointer Register Move Instructions	7 6 5 4 3 2 1 0		
XPAL	Exchange Pointer Low	0 0 1 1 0 0 ptr	$(AC)\leftrightarrow(PTR_{7:0})$	8
XPAH	Exchange Pointer High	0 0 1 1 0 1	$(AC)\leftrightarrow(PTR_{15:8})$	8
XPPC	Exchange Pointer with PC	0 0 1 1 1 1	(PC)↔(PTR)	7
	Shift, Rotate, Serial I/O Instructions	7 6 5 4 3 2 1 0		
SIO	Serial Input/Output	0 0 0 1 1 0 0 1	$(E_i)\rightarrow(E_{i-1})$, SIN→$(E_7)$, (E_0)→SOUT	5
SR	Shift Right	0 0 0 1 1 1 0 0	$(AC_i)\rightarrow(AC_{i-1})$, 0→$(AC_7)$	5
SRL	Shift Right with Link	0 0 0 1 1 1 0 1	$(AC_i)\rightarrow(AC_{i-1})$, (CY/L)→$(AC_7)$	5
RR	Rotate Right	0 0 0 1 1 1 1 0	$(AC_i)\rightarrow(AC_{i-1})$, $(AC_0)\rightarrow(AC_7)$	5
RRL	Rotate Right with Link	0 0 0 1 1 1 1 1	$(AC_i)\rightarrow(AC_{i-1})$, (AC_0)→(CY/L)→(AC_7)	5
	Single Byte Miscellaneous Instructions	7 6 5 4 3 2 1 0		
HALT	Halt	0 0 0 0 0 0 0 0	Pulse H flag	8
CCL	Clear Carry/Link	0 0 0 0 0 0 1 0	(CY/L)←0	5
SCL	Set Carry/Link	0 0 0 0 0 0 1 1	(CY/L)←1	5
DINT	Disable Interrupt	0 0 0 0 0 1 0 0	(IE)←0	6
IEN	Enable Interrupt	0 0 0 0 0 1 0 1	(IE)←1	6
CSA	Copy Status to AC	0 0 0 0 0 1 1 0	(AC)←(SR)	5
CAS	Copy AC to Status	0 0 0 0 0 1 1 1	(SR)←(AC)	6
NOP	No Operation	0 0 0 0 1 0 0 0	None	5

TABLE 3 Instruction Execution Times

INSTRUCTION	READ CYCLES	WRITE CYCLES	TOTAL MICROCYCLES	INSTRUCTION	READ CYCLES	WRITE CYCLES	MICROCYCLES
ADD	3	0	15	JP	3	0	9, 11 for Jump
ADE	1	0	7	JZ	2	0	9, 11 for Jump
ADI	2	0	11	LD	3	0	10
AND	3	0	10	LDE	1	0	6
ANE	1	0	6	LDI	3	0	10
ANI	2	0	10	NOP	1	0	5
CAD	3	0	20	OR	3	0	10
CAE	1	0	6	ORI	2	0	10
CAI	2	0	12	OTI	2	0	10
CAS	1	0	6	RR	1	0	5
CCL	1	0	5	RRL	1	0	5
CSA	1	0	5	SCL	1	0	5
DAD	3	0	23	SIO	1	0	5
DAE	1	0	11	SR	1	0	5
DAI	2	0	15	SRL	1	0	5
DINT	1	0	6	ST	2	1	10
ILD	3	1	22	XAE	1	0	7
ILY	2	0	13 - 131903	XDR	3	0	10
HALT	2	0	6	XPAH	1	0	8
IEN	1	0	6	XPAL	1	0	8
LD	3	1	22	XPPC	1	0	7
JMP	3	0	11	XRI	2	0	10
JNZ	2	0	9, 11 for Jump	XRI	2	0	10

Note: If three memory cycles are required, the appropriate value may be added to obtain the exact read or write cycle.

TABLE 4 Symbols and Notations Used to Express Instruction Execution

SYMBOL AND NOTATION	MEANING
AC	8 bit Accumulator
CY/L	Carry/Link Flag in the Status Register.
data	Signed, 8 bit immediate data field
disp	Displacement, represents an operand in a nonmemory reference instruction or an address modifier field in a memory reference instruction. It is a signed two's complement number.
EA	Effective Address as specified by the instruction.
E	Extension Register, provides for temporary storage, variable displacements and also as serial input output port
-	Unspecified bit of a register.
IE	Interrupt Enable Flag
m	Mode bit used in memory reference instructions. Blank operator sets m = 0, @ sets m = 1.
OV	Overflow Flag in the Status Register.
PC	Program Counter (Pointer Register 0), during address formation, PC points to the last byte of the instruction being executed
ptr	Pointer Register (ptr = 0 through 3). The register specified in byte 1 of the instruction.
ptr n m	Pointer register n, n m = 7 through 0 or 15 through 8
SIN	Serial Input pin.
SOUT	Serial Output pin
SR	8 bit Status Register.
( )	Means "contents of." For example, (EA) = contents of Effective Address.
[ ]	Means optional field in the assembler instruction format.
~	Ones complement of value to right of ~.
←	Means "replaces."
←	Means "is replaced by."
↔	Means "exchange."
@	When used in the operand field of the instruction, sets the mode bit (m) to 1 for auto-incrementing/auto-decrementing indexing.
10*	Modulo 10 addition.
A	AND operation.
V	Inclusive OR operation.
⊻	Exclusive-OR operation.
≥	Greater than or equal to.
=	Equals.
≠	Does not equal.

system implementation

Figures 9 through 11 illustrate typical SC/MP system configurations. In figure 9, SC/MP is shown interconnected to three memory devices to form a stand alone 4 device system that provides 256 words of read/write memory and 2,048 words for program storage. Figure 10 shows SC/MP interconnected to an external controller for Direct Memory Access (DMA) operation, and figure 11 illustrates a multi-processor application using SC/MP's built in logic to control bus access.

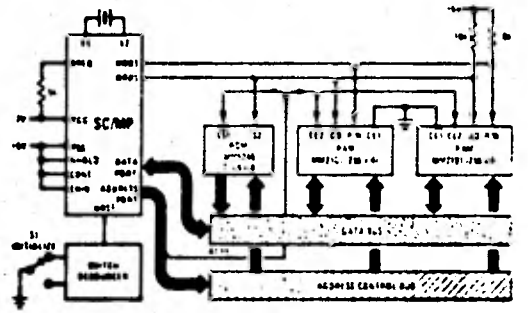


FIGURE 9 SC/MP Four Chip System

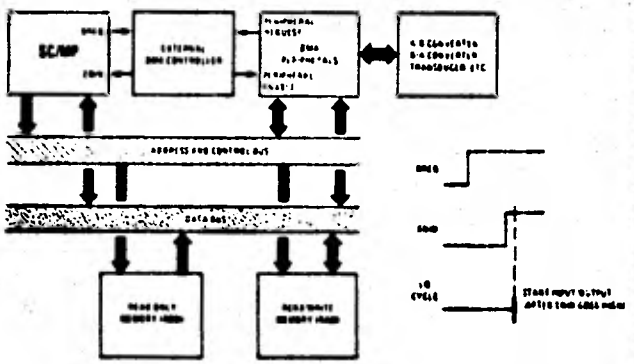


FIGURE 10. SC/MP Implementation for Direct Memory Access (DMA) Operation

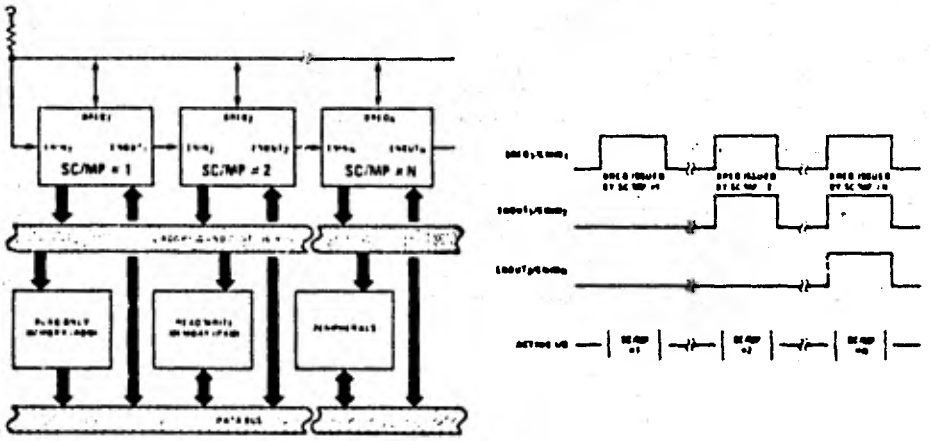
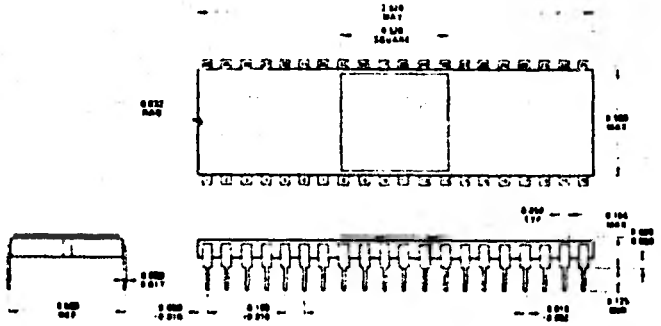


FIGURE 11. Multiprocessor System Using SC/MP Built-in Logic for Bus Control

physical dimensions



ordering information

The SC/MP device may be ordered through the local National Semiconductor sales representative or by contacting our world or international headquarters listed below. The order number is as follows:

ISP 8A/500D

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, California 95051, (408) 732-5000/TWX (910) 339-9240
National Semiconductor GmbH
808 Fuerstenfeldbruck, Industriestrasse 10, West Germany, Tele (08141) 1371/Telex 27649
National Semiconductor (UK) Ltd
Larkfield Industrial Estate, Greenock, Scotland, Tele (0475) 33251/Telex 778-632

NATIONAL

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- **Low Power — Less Than 10mW Typ. at 2MHz**
- **Operation Up to 4MHz Clock — IM6402A**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UART's — IM6402**
- **On-Chip Oscillator with External Crystal — IM6403**
- **Operating Voltage —**
  - **— IM6402-1/03-1: 4-7V**
  - **— IM6402A/03A: 4-11V**
  - **— IM6402C/03C: 5V ± 5%**

GENERAL DESCRIPTION

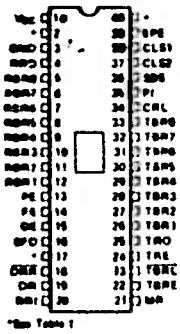
The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 7.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits operating clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 on pins 2, 17, 19, 22, and 40 as shown in Figure 5. The IM6403 utilizes pin 2 as a crystal divide control and pins 17 and 40 for an inexpensive crystal oscillator. TBREmpty and DReady are always active. All other input and output functions of the IM6402 and IM6403 are identical.

PIN CONFIGURATION



*See Table 1

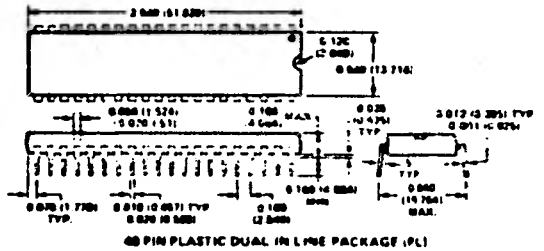
TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/ EXT CLOCK
2	N.C.	DIVIDE CONTROL	DIVIDE CONTROL
17	RRC	XTAL	EXTERNAL CLOCK INPUT
40	TRC	XTAL	GND

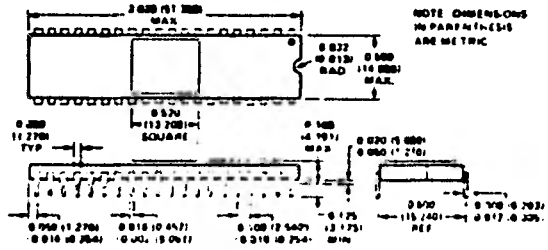
ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402C/03C
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-CPL
CERAMIC PKG	IM6402-1/03-1DL	IM6402/03-AIDL	—
MILITARY TEMP	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

PACKAGE DIMENSIONS



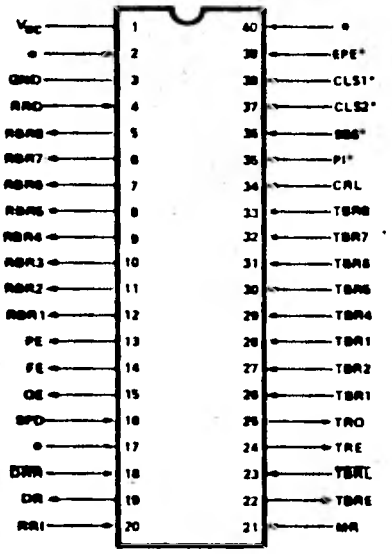
40 PIN PLASTIC DUAL IN LINE PACKAGE (PL)



40 PIN CERAMIC DUAL IN LINE PACKAGE (DL)

INTERSIL, INC., 10710 N. TANTAU AVE., CUPERTINO, CA 95014 (408) 996-5000 TWX: 910-338-0171

Printed in U.S.A.



*See Table 2 (Control Word Function)

FIGURE 1. Pin Configuration

IM6403 FUNCTIONAL PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 Divider Low: 2^{11} Divider
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state. See Figure 4.
17	IM6402-RRC IM6403-XTAL or EXT CLK IN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. 16 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 2.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR1	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR6	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 3.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL or GND	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TABLE 2. Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402AI/03AI ..... -40°C to +85°C
- Military IM6402AM/03AM ..... -55°C to +125°C

Storage Temperature ..... -65°C to 150°C
Supply Voltage ..... +12.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4V to 11V, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		5.0	500	µA
8	I_{CC}	Power Supply Current IM6402A Dynamic	f_C = 4MHz			9.0	mA
9	I_{CC}	Power Supply Current IM6403A Dynamic	$f_{CRYSTAL}$=3.58MHz			13.0	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_C	Clock Frequency IM6402A	See Timing Diagrams (Figures 2,3,4)	D.C.	6.0	4.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403A			8.0	6.0	MHz
3	t_{PW}	Pulse Widths CRL, DRR, TBRL		100	40		ns
4	t_{MR}	Pulse Width MR		400	200		ns
5	t_{DS}	Input Data Setup Time		40	0		ns
6	t_{DH}	Input Data Hold Time		30	30		ns
7	t_{EN}	Output Enable Time			40	70	ns

TIMING DIAGRAMS

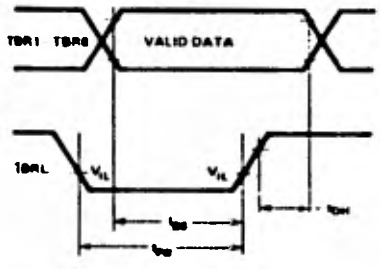


FIGURE 2. Data Input Cycle

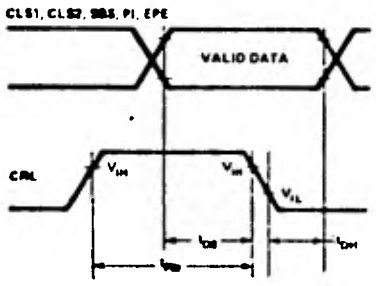


FIGURE 3. Control Register Load Cycle

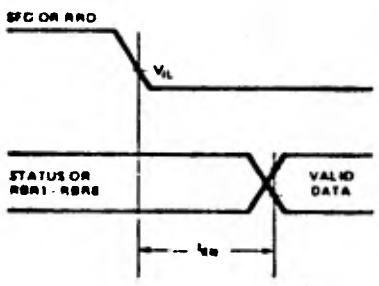


FIGURE 4. Status Flag Enable Time or Data Output Enable Time

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402-1I/03-1I ..... -40°C to +85°C
- Military IM6402-1M/03-1M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH}=-0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	100	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_C = 2MHz			1.9	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{CRYSTAL}$=3.58MHz			5.5	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_C	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.	3.0	2.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403			4.0	3.58	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
4	t_{MR}	Pulse Width MR		400	200		ns
5	t_{DS}	Input Data Setup Time		50	20		ns
6	t_{DH}	Input Data Hold Time		60	40		ns
7	t_{EN}	Output Enable Time			80	160	ns

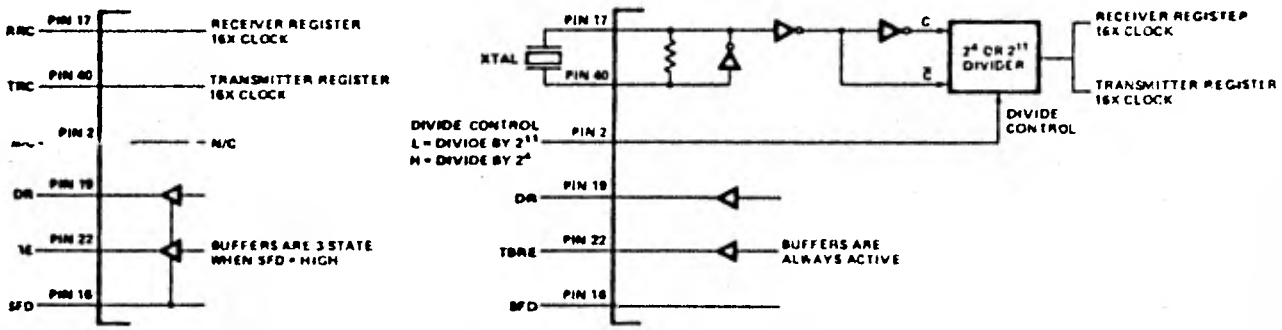


FIGURE 5. Functional Difference Between IM6402 and IM6403 UART (6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three inputs (RRC, TRC, pin 2) as shown in Figure 5. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 9). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to 2^4.

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
IM6402C/03C ..... 0°C to +70°C
Storage Temperature ..... -65°C to 150°C
Supply Voltage ..... +7.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 5% A = Commercial

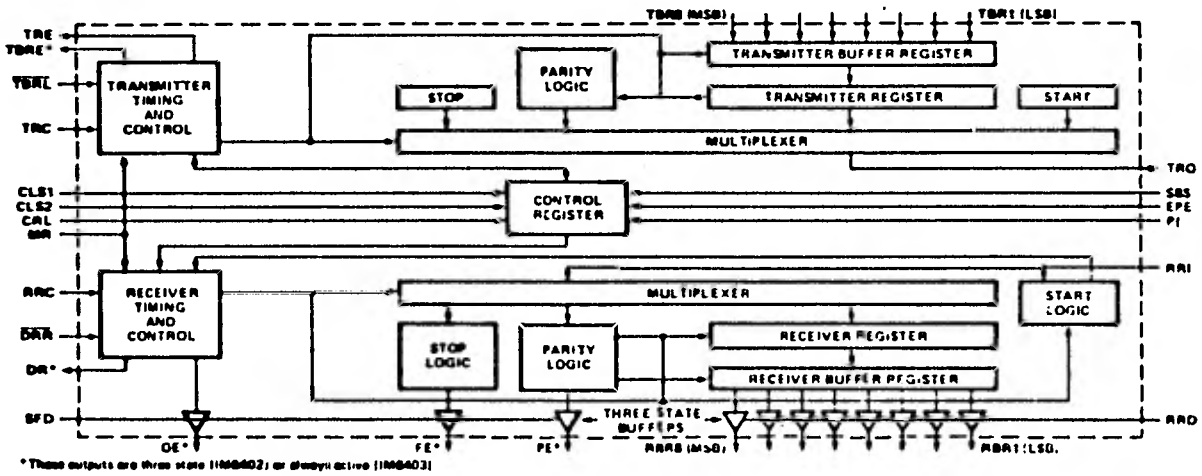
	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-1.5			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	GND<V_{IN}<V_{CC}	-5.0		5.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL}=1.6mA			0.45	V
6	I_{OL}	Output Leakage	GND<V_{OUT}<V_{CC}	-5.0		5.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	800	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_C = 500 KHz			1.2	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{CRYSTAL}$=2.46MHz			3.7	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, C_L = 50pF, T_A = Commercial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_C	Clock Frequency IM6402C	See Timing Diagrams (Figures 2,3,4)	D.C.	3.0	1.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403C			4.0	2.46	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
4	t_{MR}	Pulse Width MR		600	200		ns
5	t_{DS}	Input Data Setup Time		75	20		ns
6	t_{DH}	Input Data Hold Time		90	40		ns
7	t_{EN}	Output Enable Time			80	190	ns

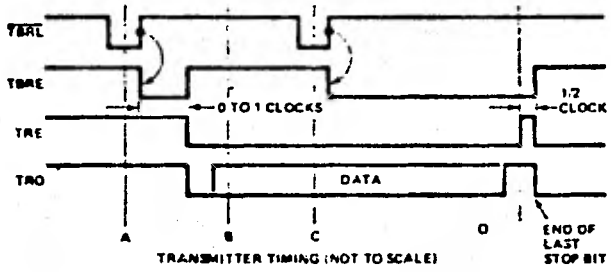


*These outputs are three state (IM6402) or always active (IM6403)

FIGURE 6. IM6402/03 Functional Block Diagram

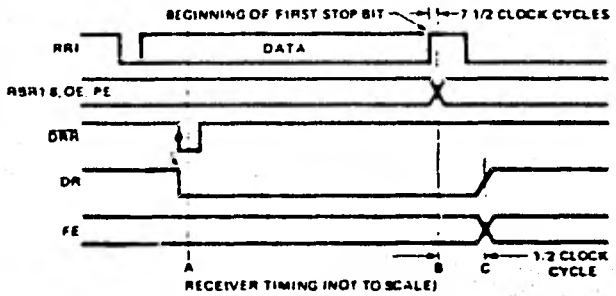
TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$oad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of $\overline{TBRL}$ clears TBREmpty. 0 to 1 clock cycles later data is transferred to the transmitter register and TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRCLock. The clock rate is 16 times the data rate. (C) A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins.



RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. (A) A low level on $\overline{DR}$Reset clears the DReady line (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. (C) 1/2 clock cycle later DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.



START BIT DETECTION

The receiver uses a 16X clock for timing. The start bit (A) could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

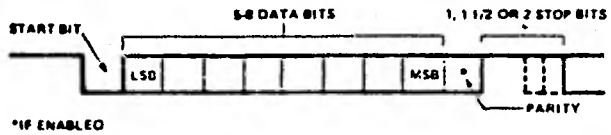
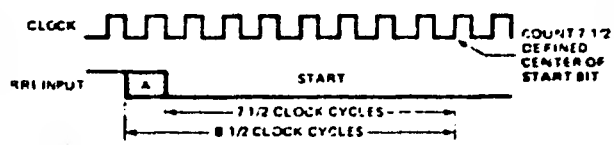


FIGURE 7. Serial Data Format



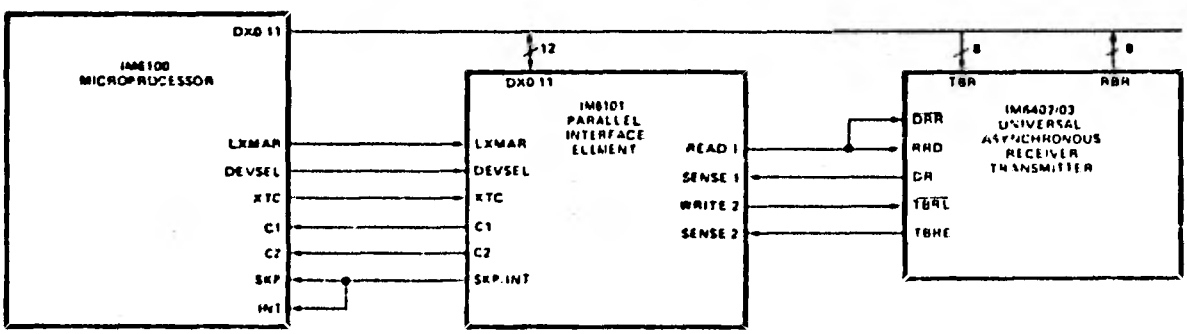


FIGURE 8. Interface Block Diagram for IM6402/03 with IM6100 Microprocessor

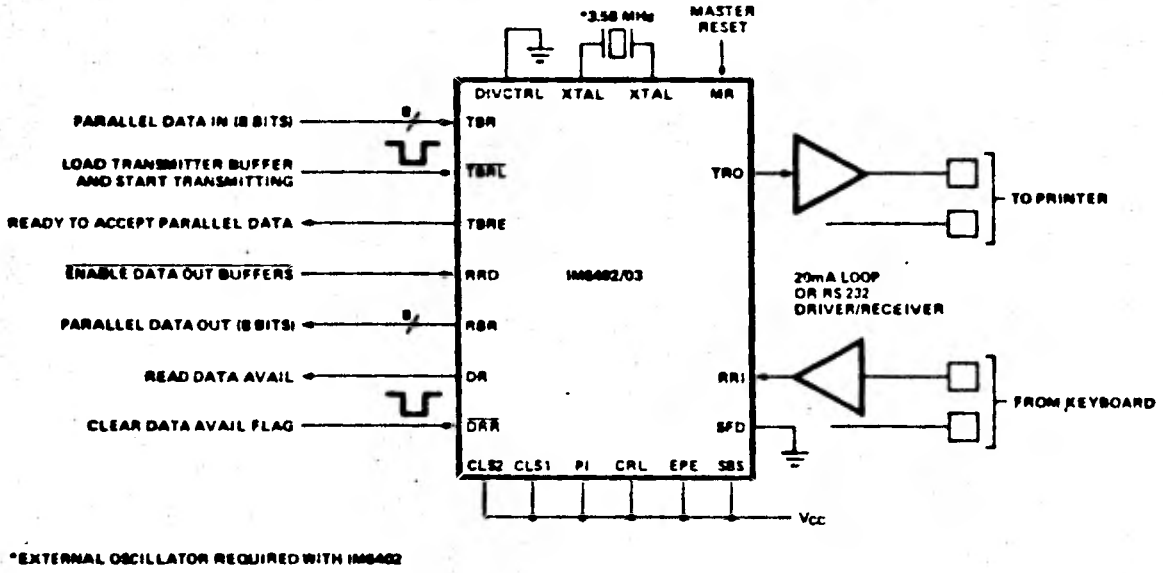


FIGURE 9. 110 Baud TTY Interface.

IB-42-30-003

INSTRUCTION MANUAL

FM DESIGNS UTILIZING PBC MODULES

RF LINK DEVICES

TRANSMITTER UNIT

810-038

Catalog No. (-01)	132-150.8 MHz
Catalog No. (-02)	150.8-162 MHz
Catalog No. (-03)	162-174 MHz
Catalog No. (-04)	66-76 MHz
Catalog No. (-05)	76-88 MHz

This RF Link unit, one of a family of modern state-of-the-art packages, utilizes 100% solid state components. Its compact design provides unusual versatility making it easily adaptable to many data communication applications. Each rugged unit is designed to handle voice and/or tone in a broad spectrum of applications.

PBC modules (Plug-in Block Circuits) have been engineered into this product to provide the ultimate in solid-state performance, reliability, durability and maintainability. These qualities give assurance that downtime will be minimized. If a circuit ever stops working, the malfunctioning module can be quickly located and replaced with a spare off-the-shelf plug-in module.

SPECIAL PRODUCTS DEPARTMENT

Repco

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ORLANDO, FLORIDA 32854

PHONE (305) 843-8484
TELEX 56-8536
TWX 810-850-0120

GENERAL SPECIFICATIONS

Frequency Range	**66-88 MHz, 132-174 MHz**
Frequency Stability	**±.0005% (-30°C to +60°C)**
RF Power Output (50 Ohm Load)	**2.2 W @ 15 VDC**
Emission Type	**15F2, 16F3**
Power Supply Volts	**+15 VDC Normal**
Operating Range	**+12.8 to +17.3 VDC**
Power Supply Current	**400 ma @ 15 VDC**
Audio Input Impedance	**5 Kilohms @ 1 KHz**
Audio Input @ 1 KHz for 3.3 KHz Deviation	**5 - 10 mv Rms**
Audio Response (300 - 3000 Hz)	**+1, -3 db of standard EIA 6 db/octave pre-emphasis characteristic**
Audio Distortion (Max)	**6% @ 2/3 rated system deviation with 1 KHz modulation**
FM Hum & Noise	**50 db below 2/3 rated system deviation**
Spurious & Harmonics	**49 db below carrier**
Weight	**3.5 oz. (99.1 grams) less external leads**
Size	**3.32" x 3.32" x 1" (2.9" x 2.9" mtg centers)**
Duty Cycle (w/o degradation)	**10% (Maximum transmission 1 minute)**

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

These Repco R. F. Link Transmitters are type accepted for domestic application in the 72-76 MHz range for 15F2 and 16F3 emission under parts 81, 87, 89, 91 and 93 of the FCC Rules and Regulations. Additionally, these Repco R. F. Link Transmitters are type accepted for domestic application in the 150.8-174 MHz range for 15F2 emission under parts 89, 91 and 93; also for 16F3 emission under parts 81, 89, 91 and 93 of the FCC Rules and Regulations. When these devices are installed in a system, it is the end user's responsibility to obtain type acceptance/certification on the system.

CRYSTAL SPECIFICATIONS

The equipment specifications involving frequency stability are assured only if crystals are supplied by the manufacturer or furnished by manufacturer approved suppliers.

23-10-006 TRANSMITTER CRYSTAL 66-88 MHz, 132-174 MHz (Y1)

Similar to military type CR-78/U (parallel resonant) except:

Case: HC-25/U except pin length .187 .010 inch

Load capacity: 20 pF

Frequency tolerance: ±.002% @ 25°C

Temperature characteristics: ±.0005% maximum shift from frequency at 25°C over range of -20°C to +60°C

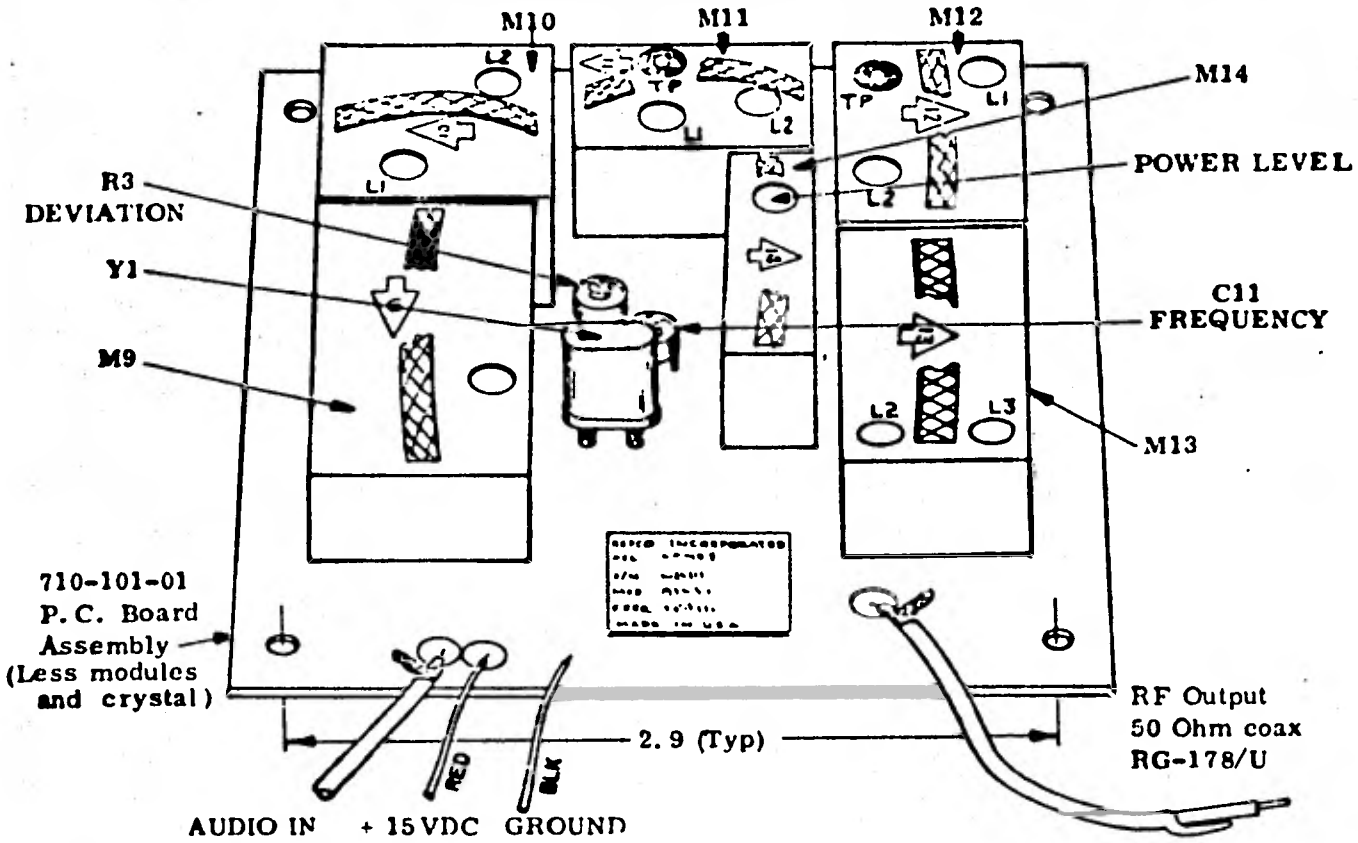
(66 - 88 MHz) 7.333333 - 9.777778
Calculate as follows to six places:

$$\text{Crystal frequency} = \frac{\text{operating frequency}}{9}$$

(132-174 MHz) 7.333333 - 9.666667
Calculate as follows to six places:

$$\text{Crystal frequency} = \frac{\text{operating frequency}}{18}$$

MECHANICAL VIEW/ALIGNMENT PROCEDURE



Note: When replacing the coax cable, carefully strip ends to duplicate original coax for proper operation and impedance matching.

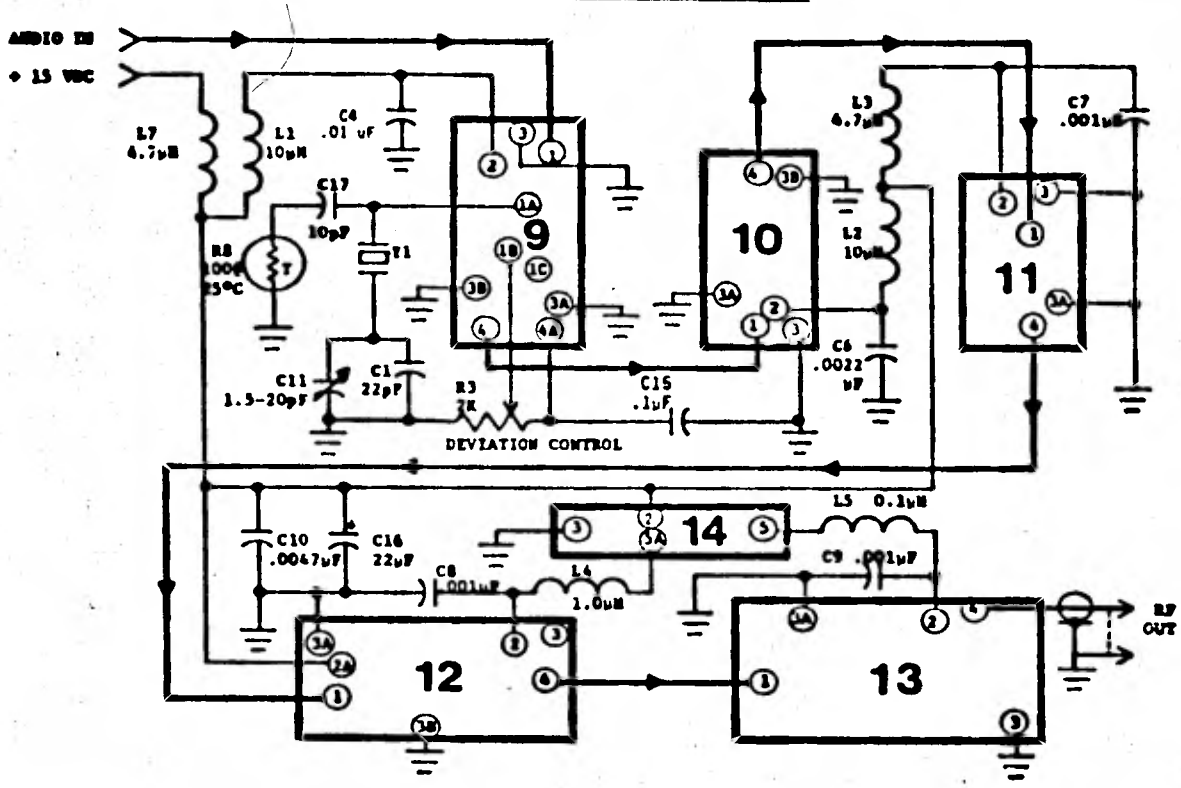
GENERAL NOTES:

1. During alignment procedures, a regulated power supply set at 15.0 volts is recommended.
2. The power should be turned off before removing and replacing modules.
3. Use only insulated type tuning tools. (order part number 510-183-01)

STEP	EVENT	INDICATING METER	ADJUSTMENT TO BE MADE	NOTES
1	Adjust 1st tripler, 2nd tripler input.	DC volt meter to test point on module #11. METER NEGATIVE TO GROUND	M10-L1 and M10-L2 for max. M11-L1 for minimum Repeat M10-L1 and M10-L2	Align M10-L1 & M10-L2 only as shown in step 1. Do not readjust in later steps while observing power levels.
2	Adjust 2nd tripler, Driver input	DC volt meter to test point on module #12 meter negative to ground.	M11-L2 for max, M12-L1 for min. M11-L1 for max. Repeat M11-L2 for max, M12-L1 for min	Do not retune M10-L1 and M10-L2 using meter indication of this step.
3	Adjust Driver, RF Amplifier	RF power output meter connected to RF load	M13-L2, M13-L3 and M12 L2 for max. Repeat	
4	Repeat Steps 1, 2 and 3			
5	Adjust RF power level	RF power output meter connected to RF load	"POWER LEVEL" to rated output power. Readjust M13-L2, M13-L3 and M12-L2 for max Repeat.	If power output does not exceed rated power at full CCW position, set the control to a position about 15° CCW from where power reduction begins.
6	Adjust Deviation Limit. Feed 0.1 VAC at 600 Hz into "AUDIO IN".	Deviation meter connected to load	"DEVIATION" (R3) control to ±5 KHz.	
7	Frequency Adjustment	Frequency meter connected to load	"FREQUENCY" (C11) to oper. freq. within ±100 Hz.	No Modulation

WARNING: FCC Rules require the person adjusting this transmitter to hold a first or second class commercial license.

TRANSMITTER SCHEMATIC



-06	-04	-03	-02	-01	ITEM NUMBER	PART NUMBER	DESCRIPTION
1	1	1	1	1	C1	15-01-006	Capacitor, Ceramic 22 pF ±10%
1	1	1	1	1	C4	15-01-043	Capacitor, Ceramic .01 uF
1	1	1	1	1	C6	15-01-032	Capacitor, Ceramic .0022 uF
2	2	2	2	2	C7, C8	15-01-041	Capacitor, Ceramic .001 uF
1	1	1	1	1	C9	15-01-041	Capacitor, Ceramic .001 uF
1	1	1	1	1	C10	15-01-042	Capacitor, Ceramic .0047 uF
1	1	1	1	1	C11	15-08-019	Capacitor, Variable 4.5-20 pF
1	1	1	1	1	C15	15-01-073	Capacitor, Ceramic 0.1 uF
1	1	1	1	1	C16	15-03-012	Capacitor, Tantalum 22 uF 15V
1	1	1	1	1	C17	15-01-020	Capacitor, Ceramic 10 pF
1	1	1	1	1		510-519-02	Label, Freq.
1	1	1	1	1	M9	909-681-01 •	Module, Modulator
	1			1	M10	910-062-01	Module, 1st Tripler
1		1	1		M10	910-781-01	Module, 1st Tripler
	1			1	M11	911-062-01	Module, 2nd Tripler
1		1	1		M11	911-781-01	Module, 2nd Tripler
1					M12	912-053-01	Module, Driver
	1				M12	912-054-01	Module, Driver
				1	M12	912-062-01	Module, Doubler/Driver
			1		M12	912-071-01	Module, Doubler/Driver
		1			M12	912-081-01	Module, Doubler/Driver
1					M13	913-053-01	Module, Final Amplifier
	1				M13	913-054-01	Module, Final Amplifier
				1	M13	913-062-01	Module, Final Amplifier
		1	1		M13	913-781-01	Module, Final Amplifier
1	1	1	1	1	M14	914-182-01	Module, Current Limiter
2	2	2	2	2	L1, L2	18-01-037	Inductor, 10 uH
1	1	1	1	1	L3	18-01-036	Inductor, 4.7 uH
1	1	1	1	1	L4	18-01-004	Inductor, 1.0 uH
1	1	1	1	1	L5	18-01-032	Inductor, 0.1 uH
1	1	1	1	1	L7	18-01-043	Inductor, 4.7 uH
1	1	1	1	1	R3	47-08-006	Resistor, Variable, 2K
1	1	1	1	1	R8	47-01-001	Resistor, Thermistor, 100 ohms

•Product revision code "A" or later

IB-42-30-015

INSTRUCTION MANUAL

FM DESIGNS UTILIZING PBC MODULES

RF LINK DEVICES

RECEIVER UNIT

810-055

Catalog No. (-01)	132-150.8 MHz
Catalog No. (-02)	150.8-162 MHz
Catalog No. (-03)	162-174 MHz
Catalog No. (-04)	66-76 MHz
Catalog No. (-05)	76-88 MHz

This RF Link unit, one of a family of modern state-of-the-art packages, utilizes 100% solid state components. Its compact design provides unusual versatility making it easily adaptable to many data communication applications. Each rugged unit is designed to handle voice and/or tone in a broad spectrum of applications.

PBC modules (Plug-in Block Circuits) have been engineered into this product to provide the ultimate in solid-state performance, reliability, durability and maintainability. These qualities give assurance that downtime will be minimized. If a circuit ever stops working, the malfunctioning module can be quickly located and replaced with a spare off-the-shelf plug-in module.

Repco RF Link receivers are certificated where applicable to FCC Rules and Regulations. When these devices are installed in a system, it is the end user's responsibility to obtain system type acceptance/certification.

SPECIAL PRODUCTS DEPARTMENT

Repco

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PHONE (305) 843-8484
TELEX 56-6536
TWX 810-850-0120

GENERAL SPECIFICATIONS

Frequency Range	66-88 MHz, 132-174 MHz
Frequency Stability	± .001% (-30°C to +60°C)
RF Input Impedance	50 ohms
Sensitivity	< 0.35 uv/12 db SINAD; < 0.5 uv/20 db Quieting
Spurious & Image Rej	70 db below carrier
Noise Squelch Sensitivity	< 0.25 uv
Adj Channel Rejection	60 db (20 db Quieting) 132-174 MHz 70 db (20 db Quieting) 66-88 MHz
Modulation Acceptance	±7 KHz
Audio Response (300-3000 Hz)	+2 to -8 db of Std. EIA 6 db/octave de-emphasis curve
Audio Output Power	500 mw at less than 10% distortion
Audio Output Impedance	25 ohms resistive
Current Drain	8.0 ma @ 12 VDC (Standby); 87 ma @ 12 VDC (Receive)
DC Operating Range	12 VDC ±1.5 VDC (per EIA RS-316)
Weight	4.2 oz (119 Grams) Less External Leads
Size	3.32" x 3.32" x 1" (2.9" x 2.9" mounting centers)
Duty Cycle (w/o degradation)	Continuous

Specifications Subject To Change Without Notice.

NOTE: This receiver, is recommended for use with transmitter units 810-039, 810-040, 810-041, 810-042, 810-043, 816-011 and 816-040.

CRYSTAL SPECIFICATIONS

The equipment specifications involving frequency stability are assured only if crystals are supplied by the manufacturer or furnished by manufacturer approved suppliers.

23-10-007 Receive Crystal (Y2) Military Type CR-77/U (series resonant) except:
Case: HC-25/U except pin length .187 ±.010 inch
Dissipation: 1 milliwatt maximum
Frequency Tolerance at 25°C: ±.001%
Temperature Data: ±.0008% max. shift from freq. at +25°C over -30°C to +60°C range

Crystal frequency is calculated to six places as follows:

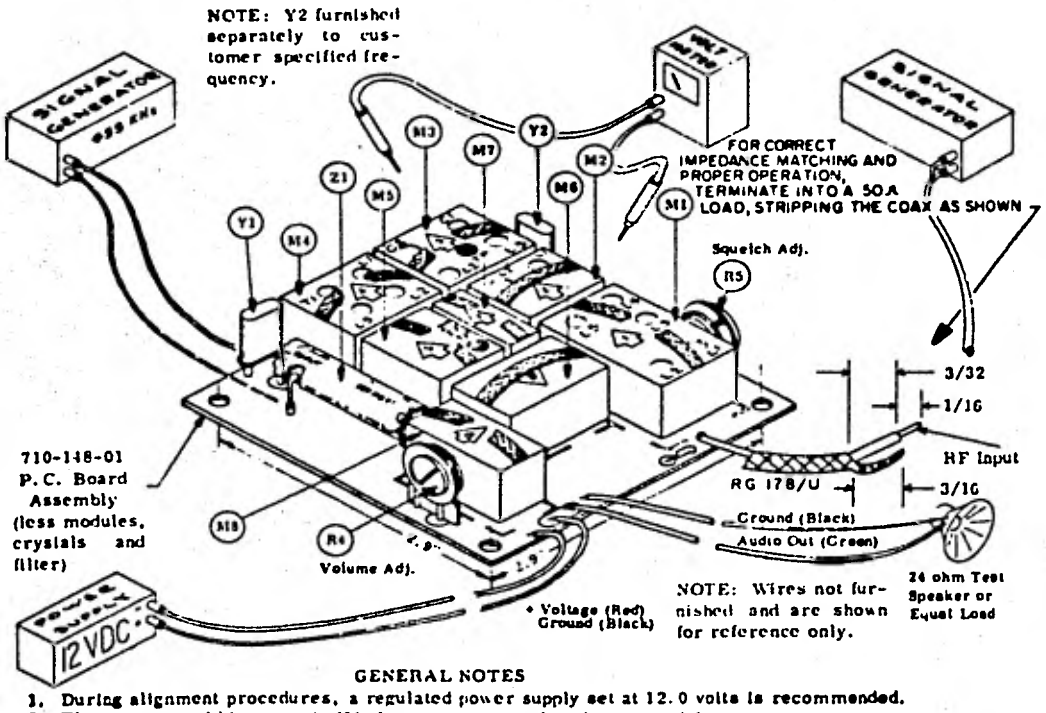
$$\frac{\text{66-88 MHz operating frequency plus 10.7 MHz}}{2} = \text{Crystal frequency (38.350000 - 49.350000 MHz)}$$

$$\frac{\text{132.150.8 MHz operating frequency plus 10.7 MHz}}{3} = \text{Crystal frequency (47.566666 - 53.833333 MHz)}$$

$$\frac{\text{150.8-174 MHz operating frequency minus 10.7 MHz}}{3} = \text{Crystal frequency (46.700000 - 54.433333 MHz)}$$

23-09-002 Receiver Second Oscillator Crystal (Y1) Military Type CR-78/U parallel resonant) except
Case: HC-25/U except pin length .187 ±.010 inch
Frequency: 10.245 MHz ±.003% at 25°C
Load Capacity: 68 pF
Temperature Data: ±.002% max. shift from freq. at +25°C over -30°C to +60°C range

NOTE: Some units utilize receiver second oscillator crystals with frequency specifications of 10.243 MHz (23-09-005, coded blue) or 10.217 MHz (23-09-004, coded orange). In these cases the IF filters (Z1) have compatible band pass characteristics and are provided with a matching color code.



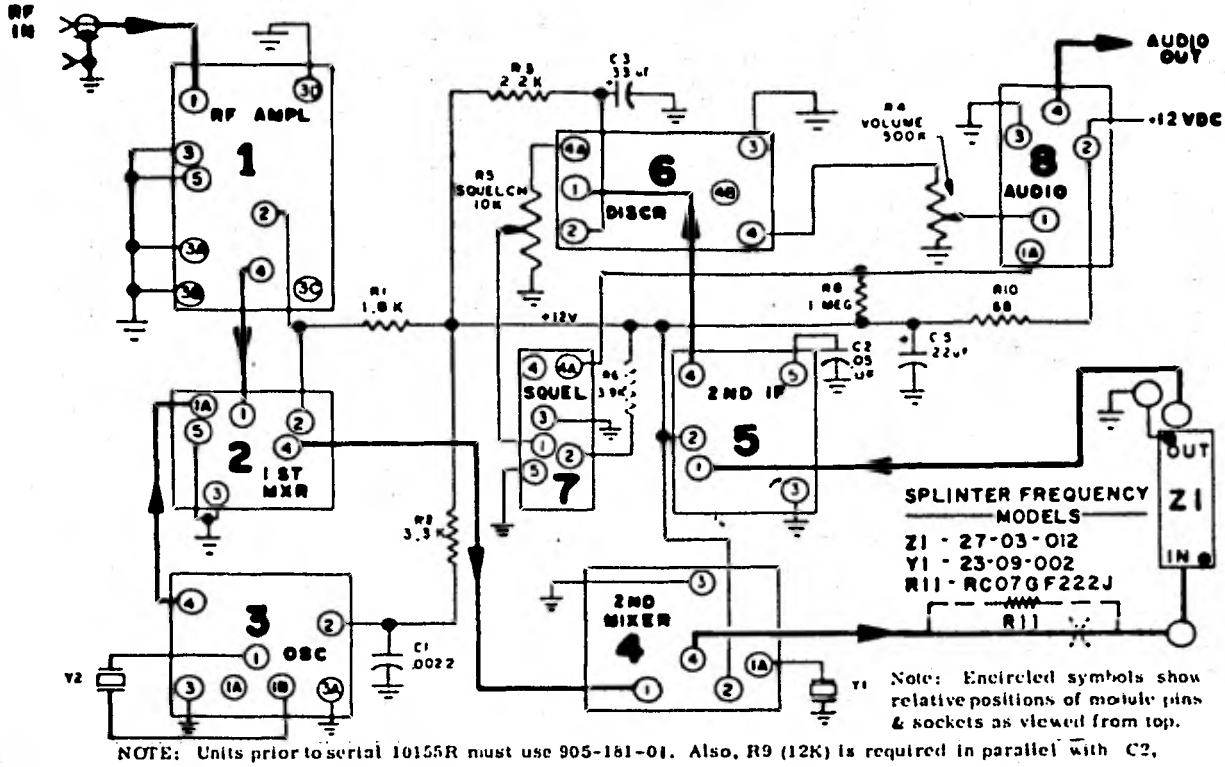
GENERAL NOTES

1. During alignment procedures, a regulated power supply set at 12.0 volts is recommended.
2. The power should be turned off before removing and replacing modules.
3. Use only insulated type tuning tools. (order part number 510-163-01).
4. There are no adjustments or test points for the pulse - averaging discriminator used in this receiver.

STEP	TEST EQUIPMENT AND CONNECTIONS INPUT	OUTPUT	ADJUST	NOTES
1	None	Electronic voltmeter (VTVM) DC probe to test point on M3. Ground other lead.	Adjust M3-L2 for maximum voltage. Adjust M3-L3 for minimum reading.	
2	Tune Signal generator to exact channel frequency and connect to "RF In" (antenna co-ax).	Electronic voltmeter (VTVM) DC probe to test point on M5. Ground other lead.	In order, tune the following: M1-L4, M1-L5, M1-L3, M1-L2, M1-L1, M2-L1, M2-L2, M4-L1, M4-L2, M4-L3, M4-T1. Readjust if necessary.	Adjust signal generator level so that meter remains in a 0.3 to 0.5 volt range.
3	Acquire your precise channel frequency from either a base station or signal generator, then loosely couple a 455 Kilz signal into the input side of the filter (Z1)	Look for zeroing of the meter or listen for audio zero beat in test speaker.	Adjust M3-C2 to obtain zero beat and maximum quieting. (M3-C1 is inactive)	If filter Z1 and Crystal Y1 have color code other than green, use 453.5 Kilz for units coded orange and 456.5 Kilz for units coded blue.
4	Same as Step 2	Same as Step 2	Fine adjustment of M1-L1 and M1-L2.	

*M4-L3 adjustment has been eliminated on module 904-181 with revision code "A" or later.

SCHEMATIC (SERIAL 10155R AND UP)



Note: Encircled symbols show relative positions of module pins & sockets as viewed from top.

NOTE: Units prior to serial 10155R must use 905-181-01. Also, R9 (12K) is required in parallel with C2, R1 is 2.7K, R2 is 4.7K and R3 is 1.5K.

NOTE: With CTCSS tone decoder, the following outputs are used: M7P1 - squelch output (0.8 VDC) and M6 pin 4 B - discriminator output.

810-055 -05	-04	-03	-02	-01	ITEM NO.	PART NUMBER	DESCRIPTION
-	1	-	-	-	M1	901-051-01	Module, RF Amplifier
1	-	-	-	-	M1	901-053-01	Module, RF Amplifier
-	-	-	-	1	M1	901-061-01	Module, RF Amplifier
-	-	-	1	-	M1	901-071-01	Module, RF Amplifier
-	-	1	-	-	M1	901-081-01	Module, RF Amplifier
1	1	1	1	1	M2	902-181-01	Module, First Mixer
1	1	-	-	-	M3	903-051-01	Module, First Oscillator
-	-	1	1	1	M3	903-681-01	Module, First Oscillator
1	1	1	1	1	M4	904-181-01	Module, 2nd Mixer/Oscillator
1	1	1	1	1	M5	905-185-01	Module, 2nd IF Amplifier
1	1	1	1	1	M6	906-181-01	Module, Discriminator
1	1	1	1	1	M7	907-181-01	Module, Squelch (code B or later)
1	1	1	1	1	M8	908-181-01	Module, Receive Audio
1	1	1	1	1	Y1	23-09-002	Crystal, 10.245 Mhz
1	1	1	1	1	Y2	23-10-007	Crsytal, 1st Oscillator
1	1	1	1	1	Z1	710-052-04	Filter, 455 Khz
1	1	1	1	1	C1	15-01-033	Capacitor, .0022 uF
1	1	1	1	1	C2	15-01-007	Capacitor, 0.05 uF
1	1	1	1	1	C3	15-03-026	Capacitor, 33 uF
1	1	1	1	1	C5	15-03-012	Capacitor, 22 pF
1	1	1	1	1	R1	47-13-182	Resistor, 1.8K 5% 1/4W
1	1	1	1	1	R2	47-13-332	Resistor, 3.3K 5% 1/4W
1	1	1	1	1	R3	47-13-222	Resistor, 2.2K 5% 1/4W
1	1	1	1	1	R4	47-08-017	Resistor, Variable, 500K
1	1	1	1	1	R5	47-08-016	Resistor, Variable, 10K
1	1	1	1	1	R6	47-13-392	Resistor, 3.9K 5% 1/4W
1	1	1	1	1	R8	RC05GF1051	Resistor, 1 MEG 5% 1/8W
1	1	1	-	1	R10	47-13-680	Resistor, 68 5% 1/4W

3C78300

XR-2206

Monolithic Function Generator

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The XR-2206 is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000: 1 frequency range with an external control voltage with very little affect on distortion.

As shown in Figure 1, the monolithic circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The internal current switches transfer the oscillator current to any one of the two external timing resistors to produce two discrete frequencies selected by the logic level at the FSK input terminal (pin 9).

FEATURES

- Low Sinewave Distortion (THD .5%) — insensitive to signal sweep
- Excellent Stability (20 ppm/°C, typ)
- Wide Sweep Range (2000:1, typ)
- Low Supply Sensitivity (0.01%/V, typ)
- Linear Amplitude Modulation
- Adjustable Duty-Cycle (1% to 99%)
- TTL Compatible FSK Controls
- Wide Supply Range (10V to 26V)

APPLICATIONS

- Waveform Generation
  - Sine, Square, Triangle, Ramp
- Sweep Generation
- AM/FM Generation
- FSK and PSK Generation
- Voltage-to-Frequency Conversion
- Tone Generation
- Phase-Locked Loops

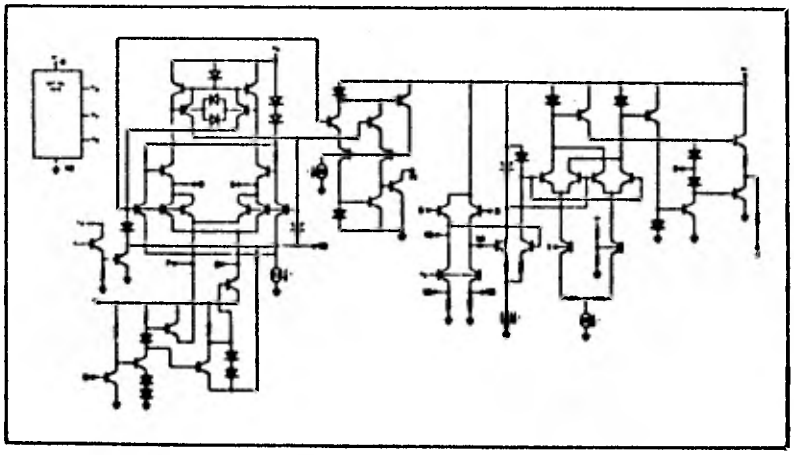
ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Plastic package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

AVAILABLE TYPES

Part Number	Package Types	Operating Temperature Range
XR-2206M	Ceramic	−55°C to +125°C
XR-2206N	Ceramic	0°C to +75°C
XR-2206P	Plastic	0°C to +75°C
XR-2206CN	Ceramic	0°C to +75°C
XR-2206CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

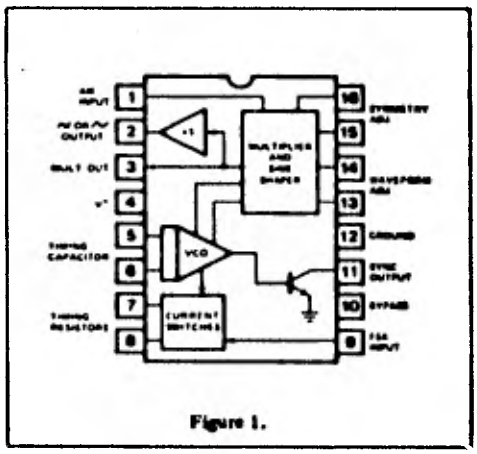


Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Fig. 2, $V^+ = 12V$, $T_A = 25°C$, $C = 0.01\ \mu F$, $R_1 = 100\ K\Omega$, $R_2 = 10\ K\Omega$ $R_3 = 25\ K\Omega$ unless otherwise specified. S_1 open for triangle, closed for sinewave.

CHARACTERISTICS	XR-2206/XR-2206M			XR-2206C			UNITS	CONDITIONS
	MIN.	TYP.	MAX	MIN.	TYP.	MAX		
Supply Voltage								
Single Supply	10		26	10		26	V	
Split Supply	±5		±13	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10\ K\Omega$
Oscillator Section								
Max. Operating Frequency	0.5	1		0.5	1		MHz	C = 1000 pF, R_1 = 1 KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50 μF, R_1 = 2 MΩ
Frequency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability		±10	±50		±20		ppm/°C	$0°C \leq T_A \leq 75°C$, $R_1 = R_2 = 20\ K\Omega$
Supply Sensitivity		0.01	0.1		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2 = 20\ K\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1 KΩ f_L @ R_1 = 2 MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1 kHz, f_H = 10 kHz
1000:1 Sweep		8			8		%	f_L = 100 Hz, f_H = 100 kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	μF	See Figure 5
Timing Resistors: R_1 & R_2	1		2000	1		2000	KΩ	
Triangle/Sinewave Output								See Note 1, Fig. 3
Triangle Amplitude		160			160		mV/KΩ	Fig. 2 S_1 Open
Sinewave Amplitude	40	60	80		60		mV/KΩ	Fig. 2 S_1 Closed
Max. Output Swing		6			6		Vpp	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sinewave Amplitude Stability		-4800			-4800		ppm/°C	See Note 2
Sinewave Distortion								R_1 = 30 KΩ
Without Adjustment		2.5			2.5		%	See Figure 11
With Adjustment		0.4	1.0		0.5	1.5	%	See Figure 12
Amplitude Modulation								
Input Impedance	50	100		50	100		KΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square Wave Output								Measured at Pin 11
Amplitude		12			12		Vpp	
Rise Time		250			250		nsec	C_L = 10 pF
Fall Time		50			50		nsec	C_L = 10 pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	I_L = 2 mA
Leakage Current		0.1	20		0.1	100	μA	V_{11} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See Section on Circuit Controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output Amplitude is directly proportional to the resistance R_3 on Pin 3. See Figure 3.
Note 2: For maximum amplitude stability R_3 should be a positive temperature coefficient resistor.

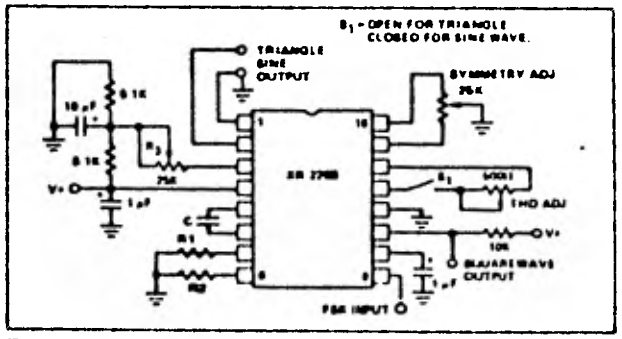


Figure 2. Basic Test Circuit

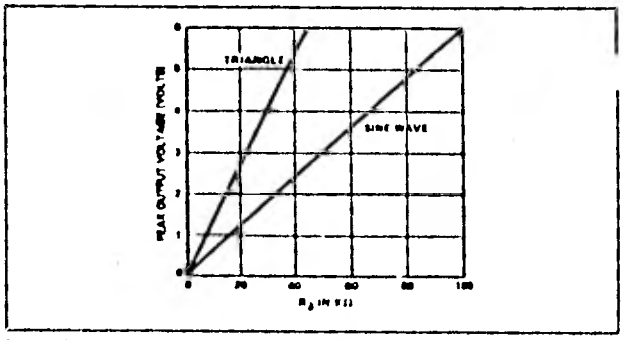


Figure 3. Output Amplitude as a Function of Resistor R_3 at Pin 3.

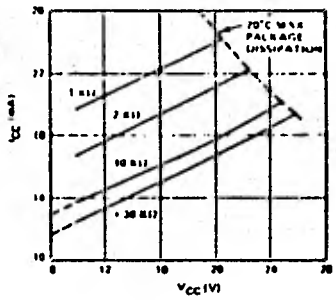


Figure 4. Supply Current vs Supply Voltage, Timing R

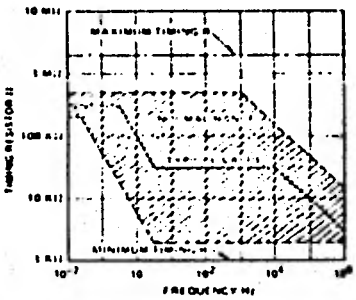


Figure 5. R vs Oscillation Frequency

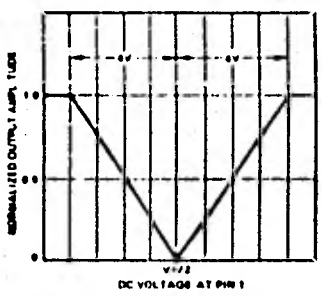


Figure 6. Normalized Output Amplitude vs DC Bias at AM Input (Pin 1).

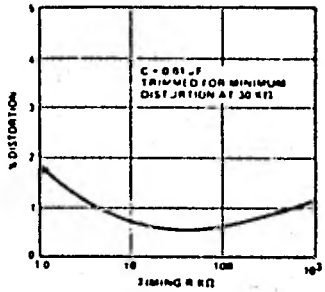


Figure 7. Trimmed Distortion vs Timing Resistor

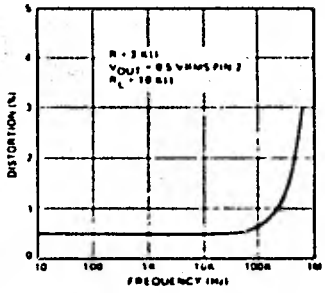


Figure 8. Signwave Distortion vs Operating Frequency With Timing Capacitors Varied

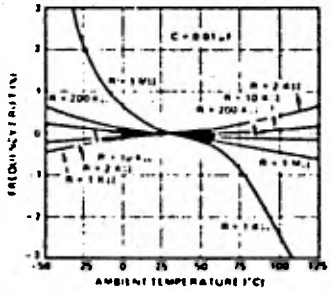


Figure 9. Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

FREQUENCY OF OPERATION:

The frequency of oscillation, f_o, is determined by the external timing capacitor C across pins 5 and 6, and by the timing resistor R connected to either pin 7 or pin 8. The frequency is given as

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R for a given frequency range are shown in Figure 5. Temperature-stability is optimum for $4\ K\Omega < R < 200\ K\Omega$. Recommended values of C are from 1000 pF to 100 μF.

FREQUENCY SWEEP AND MODULATION

Frequency of oscillation is porportional to the *total* timing current I_T drawn from pin 7 or 8

$$f = \frac{3201_T\,(mA)}{C\,(\mu F)} \text{ Hz}$$

Timing terminals (pins 7 or 8) are low impedance points and are internally biased at +3V, with respect to pin 12. Frequency varies linearly with I_T over a wide range of current values, from 1 μA to 3 mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in Figure 10. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC}\left[1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right] \text{ Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f/\partial V_C = -\frac{0.32}{R_C C} \text{ Hz/V}$$

NOTE: For safe operation of the circuit I_T should be limited to ≤3 mA.

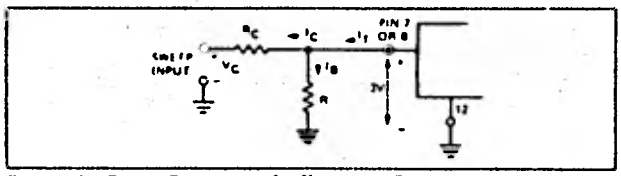


Figure 10. Circuit Connection for Frequency Sweep

OUTPUT CHARACTERISTICS:

Output Amplitude: Maximum output amplitude is inversely porportional to external resistor R_3 connected to Pin 3 (See Fig. 3). For sinewave output, amplitude is approximately 60 mV peak per KΩ of R_3; for triangle, the peak amplitude is approximately 160 mV peak per KΩ of R_3. Thus, for example, R_3 = 50 KΩ would produce approximately ±3V sinusoidal output amplitude.

Amplitude Modulation: Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100 KΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ±4 volts of $V^+/2$ as shown in Fig. 6. As this bias level approaches $V^+/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

Note: AM control must be used in conjunction with a well-regulated supply since the output amplitude now becomes a function of V^+.

FREQUENCY-SHIFT KEYING

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing pins 7 and 8, respectively, as shown in Figure 13. Depending on the polarity of the logic signal at pin 9, either one or the other of these timing

resistors is activated. If pin 9 is open-circuited or connected to a bias voltage $\geq$ 2V, only R_1 is active. Similarly, if the voltage level at pin 9 is $\leq$ 1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2 as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at pin 9 is referenced to V^-.

OUTPUT DC LEVEL CONTROL

The dc level at the output (pin 2) is approximately the same as the dc bias at pin 3. In Figures 11, 12 and 13, pin 3 is biased mid-way between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

SINEWAVE GENERATION

A) Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer R_1 at pin 7 provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$ and the

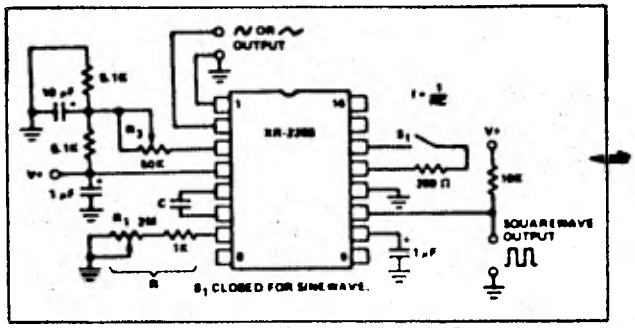


Figure 11. Circuit for Sinewave Generation Without External Adjustment. (See Fig. 3 for choice of R_3)

typical distortion (THD) is < 2.5%. If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split supply operation simply by replacing all ground connections with V^-. For split supply operation, R_3 can be directly connected to ground.

B) With External Adjustment

The harmonic content of sinusoidal output can be reduced to ≈0.5% by additional adjustments as shown in Figure 12. The potentiometer R_A adjusts the sine-shaping resistor; and R_B provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at mid-point and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

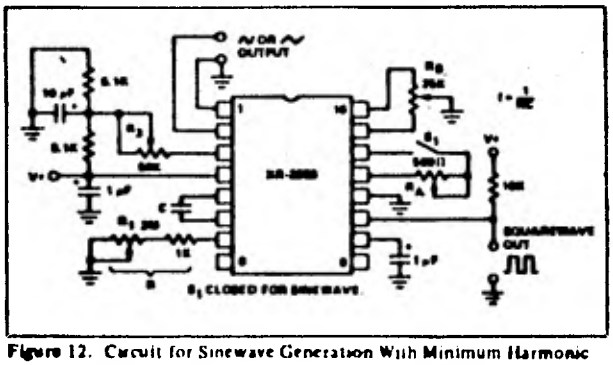


Figure 12. Circuit for Sinewave Generation With Minimum Harmonic Distortion. (R_3 Determines output Swing – See Fig. 3)

TRIANGLE WAVE GENERATION

The circuits of Figures 11 and 12 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sinewave output.

FSK GENERATION

Figure 13 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors R_1 and R_2; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-.

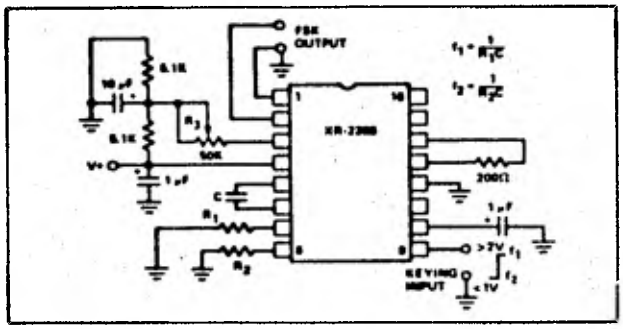


Figure 13. Sinusoidal FSK Generator

PULSE AND RAMP GENERATION

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1 KΩ to 2 MΩ.

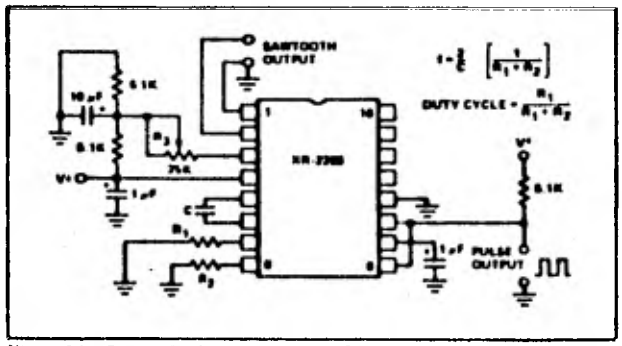


Figure 14. Circuit for Pulse and Ramp Generation

XR-2211

FSK Demodulator/Tone Decoder

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier-Detection	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

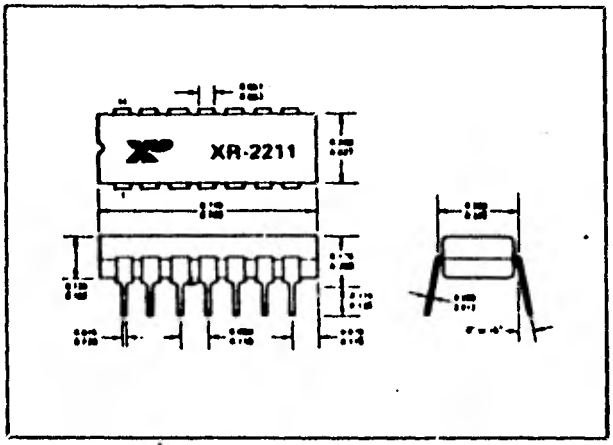
ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5.0 mW/°C

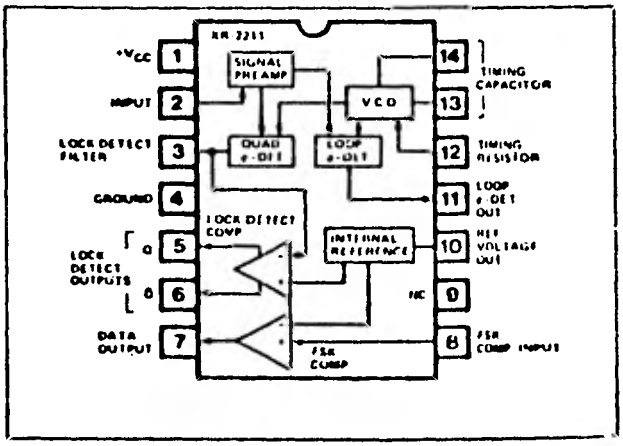
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	-55°C to +125°C
XR-2211CN	Ceramic	0°C to +75°C
XR-2211CP	Plastic	0°C to +75°C
XR-2211N	Ceramic	-40°C to +85°C
XR-2211P	Plastic	-40°C to +85°C

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30\ K\Omega$, $C_0 = 0.033\ \mu F$. See Fig. 2 for component designation

CHARACTERISTICS	XR-2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Current		4	7		5	9	mA	$R_0 \geq 10\ K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$. See Fig. 7.
		0.2			0.2		%/V	$V^+ = 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ K\Omega$, $C_0 = 400\ pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		μA	
Output Impedance		1			1		MΩ	
Maximum Swing		11			11		Vpp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		KΩ	
Input Signal								
Voltage Required to Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTIONS								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ K\Omega$
Output Voltage Low		300			300		mV	$I_C = 3\ mA$
Output Leakage Current		.01			.01		μA	$V_O = 12V$
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	

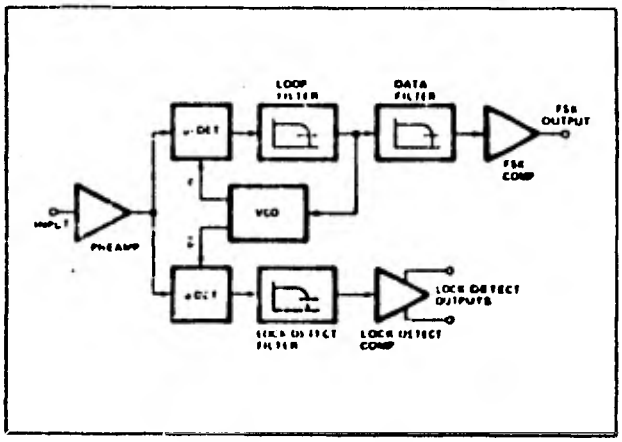


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

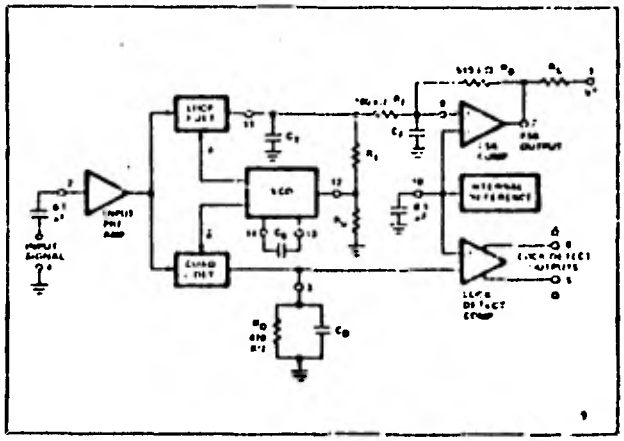


Figure 2. Generalized Circuit Connection for FSK and Tone Detection.

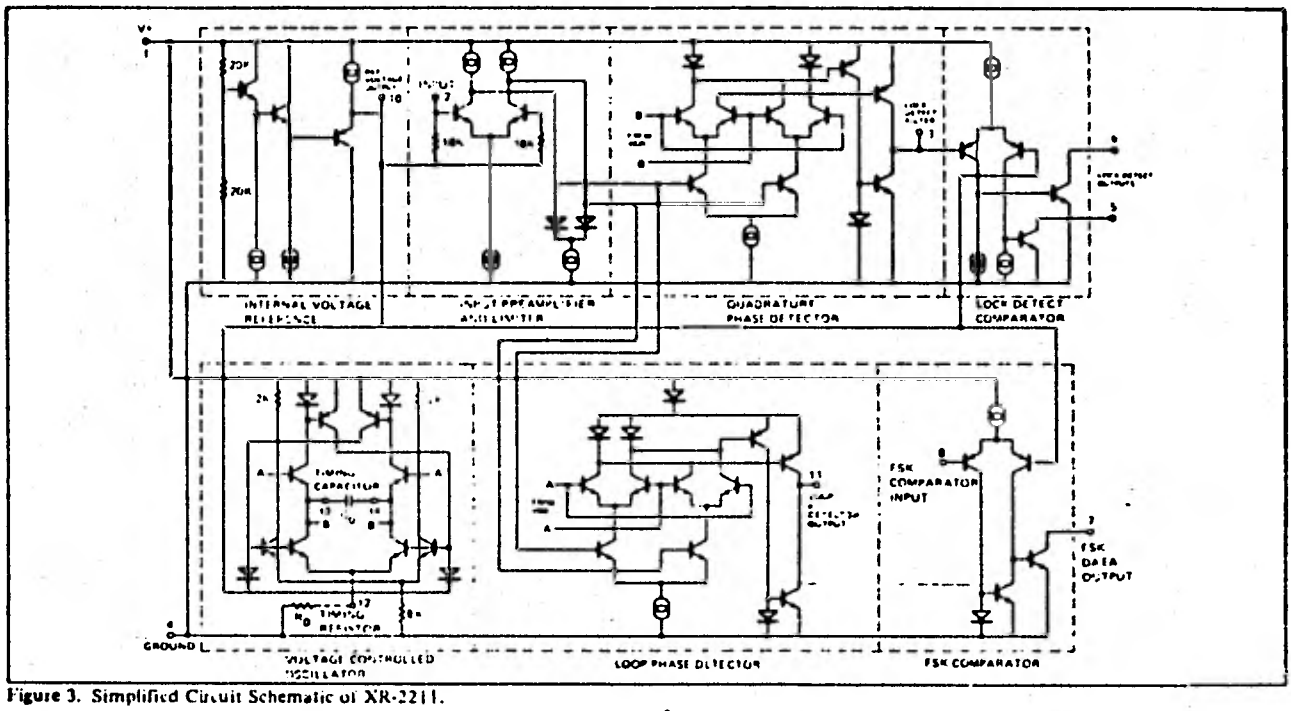


Figure 3. Simplified Circuit Schematic of XR-2211.

TYPICAL CHARACTERISTICS

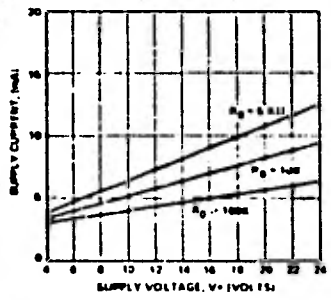


Figure 4. Typical Supply Current vs V⁺ (Logic Outputs Open Circuited).

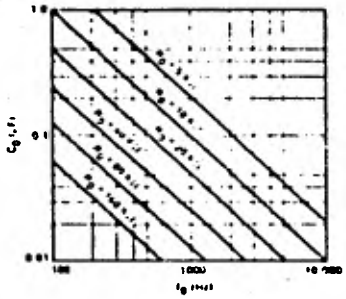


Figure 5 VCO Frequency vs Timing Resistor

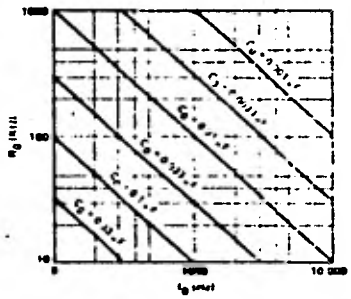


Figure 6. VCO Frequency vs Timing Capacitor

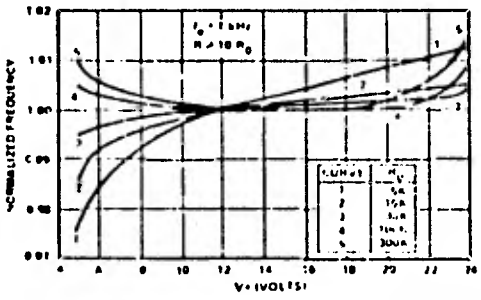


Figure 7. Typical f_0 vs Power Supply Characteristics.

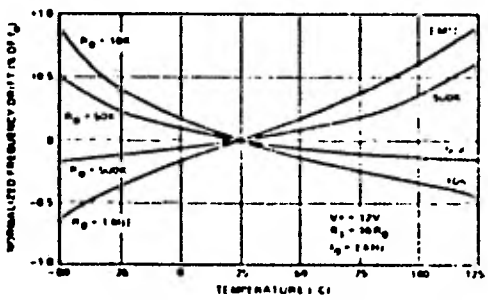


Figure 8. Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mVrms to 3 Vrms.

Quadrature Phase Detector Output (Pin 3): This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (See Fig. 2) to eliminate the chatter at lock-detect outputs. If the tone-detect section is not used, Pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

Lock-Detect Complement, $\bar{Q}$ (Pin 6): The output at Pin 6 is the logic complement of the lock-detect output at Pin 5. This output is also an open-collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open-collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency; and at "low" or on state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (Pin 11). This data filter is formed by R_F and C_F of Fig. 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 *must* be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (See Fig. 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \quad \text{Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ (See Fig. 8).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤ 3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (See Fig. 5). C_0 must be non-polar, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (See Fig. 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with C_D disconnected), with no input and with Pin 2 shorted to Pin 10.

DESIGN EQUATIONS

(See Fig. 2 for Definition of Components)

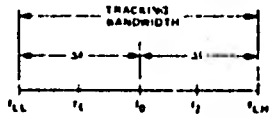
1. VCO Center Frequency, f_0:
   $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 10)
   $V_R = V+/2 - 650$ mV

3. Loop Low-Pass Filter Time Constant, τ:
   $\tau = R_1C_1$

4. Loop Damping, ζ:
   $$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τ_F:
   $\tau_F = R_FC_F$

7. Loop Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input)
   $K_\phi = -2V_R/\pi$ volts/radian

8. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):
   $K_0 = -1/V_RC_0R_1$ Hz/volt

9. Total Loop Gain, K_T:
   $K_T = 2\pi K_\phi K_0 = 4/C_0R_1$ rad/sec/volt

10. Peak Phase-Detector Current, I_A:
    $I_A = V_R$ (volts)/25 mA

APPLICATIONS INFORMATION

FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from Pin 7 to Pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table I.

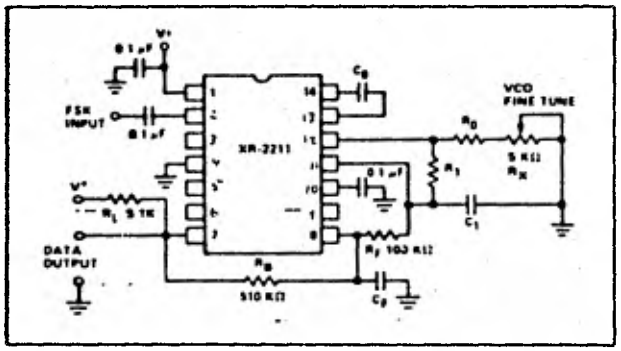


Figure 9. Circuit Connection for FSK Decoding

Design Instructions:

The circuit of Fig. 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_0:

$$f_0 = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Fig. 6:

$$C_0 = 1/R_0 f_0$$

d) Calculate R_1 to give a Δf equal to the mark-space deviation:

$$R_1 = R_0 [f_0/(f_1 - f_2)]$$

e) Calculate C_1 to set loop damping. (See Design Equation No. 4).

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

f) Calculate Data Filter Capacitance, C_F:

For R_F = 100 KΩ, R_B = 510 KΩ, the recommended value of C_F is:

$C_F \approx 3/(\text{Baud Rate})\ \mu F$

Note: All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Fig. 9).

Design Example:

75 Baud FSK demodulator with mark/space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: $f_0 = (1110 + 1170)(1/2) = 1140$ Hz
Step 2: Choose R_0 = 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer)
Step 3: Calculate C_0 from Fig. 6: $C_0 = 0.044\ \mu F$
Step 4: Calculate R_1: $R_1 = R_0(2240/60) = 380$ KΩ
Step 5: Calculate C_1: $C_1 = C_0/4 = 0.011\ \mu F$

Note: All values except R_0 can be rounded-off to *nearest* standard value.

FSK BAND	COMPONENT VALUES
300 Baud f_1 = 1070 Hz f_2 = 1270 Hz	C_0 = 0.039 µF C_F = 0.005 µF C_1 = 0.01 µF R_0 = 18 KΩ R_1 = 100 KΩ
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	C_0 = 0.022 µF C_F = 0.005 µF C_1 = 0.0047 µF R_0 = 18 KΩ R_1 = 200 KΩ
1200 Baud f_1 = 1200 Hz f_2 = 2200 Hz	C_0 = 0.027 µF C_F = 0.0022 µF C_1 = 0.01 µF R_0 = 18 KΩ R_1 = 30 KΩ

TABLE I

Recommended Component Values for Commonly Used FSK Bands (See Circuit of Fig. 9)

FSK DECODING WITH CARRIER-DETECT:

The lock-detect section of XR-2211 can be used as a carrier-detect option, for FSK decoding. The recommended circuit connection for this application is shown in Fig. 10. The open-collector lock-detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PPL, and the Pin 6 output goes "high", to enable the data output.

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_c > \Delta f/2$. For R_D = 470 KΩ, the approximate minimum value of C_D can be determined by:

$C_D\ (\mu F) \geq 16/\text{capture range in Hz.}$

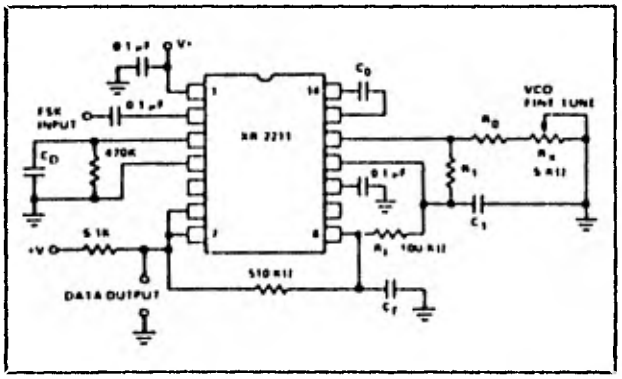


Figure 10. External Connections for FSK Demodulation with Carrier-Detect Capability.
Note: Data Output is "Low" When No Carrier is Present.

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of C_D will slow the response time of the lock-detect output.

TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\bar{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at Pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Fig. 11.

With reference to Figs. 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\bar{Q}$ logic outputs.

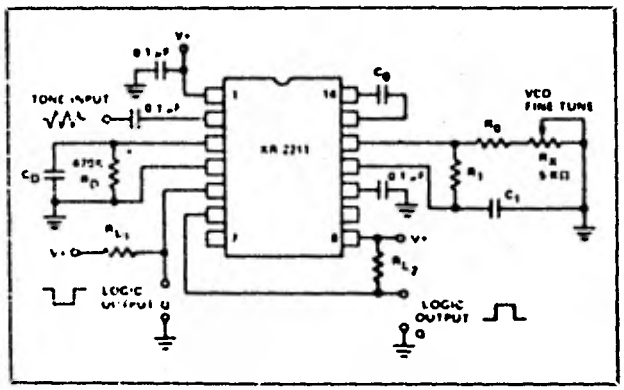


Figure 11. Circuit Connection for Tone Detection

Design Instructions:

The circuit of Fig. 11 can be optimized for any tone-detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_S: (See Fig. 6). $C_0 = 1/R_0 f_S$

c) Calculate R_1 to set bandwidth $\pm\Delta f$: (see design Equation No. 5):

$$R_1 = R_0(f_0/\Delta f)$$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor:

$$C_1 = C_0/16\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving $C_1 = 0.25\ C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with $R_D = 470$ KΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz ± 20 Hz:

a) Choose $R_0 = 20$ KΩ (18 KΩ in series with 5 KΩ potentiometer).
b) Choose C_0 for $f_0 = 1$ kHz: From Fig. 6: $C_0 = 0.05$ µF.
c) Calculate R_1: $R_1 = (R_0)(1000/20) = 1$ MΩ.
d) Calculate C_1: for $\zeta = 1/2$, $C_1 = 0.25$, $C_0 = 0.013$ µF.
e) Calculate C_D: $C_D = 16/38 = 0.42$ µF.
f) Fine-tune center frequency with 5 KΩ potentiometer, R_X.

ADJUSTMENT PROCEDURE

With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_0 can be monitored:

1. Short pin 2 to pin 10 and measure f_0 at pin 3 with C_D disconnected;
2. Open R_1 and monitor pin 13 or 14 with a high-impedance probe; or
3. Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

NOTE: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

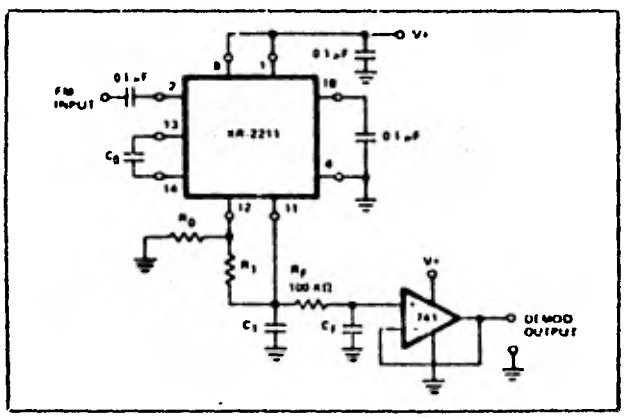


Figure 12. Linear FM Detector Using XR-2211 and an External Op. Amp. (See section on Design Equations, for Component Values)

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Fig. 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Fig. 12.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{out} = R_1\ V_R/100\ R_0 \text{ Volts/\%deviation}$$

where V_R is the internal reference voltage, ($V_R \approx V+/2 - 650$ mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on Design Equations.

AUGUST 1975

NATIONAL

MM4204/MM5204
electrically programmable 4096-bit read only memory (EROM)

MM4204/MM5204
electrically programmable 4096-bit read only memory (EROM)

general description

The MM4204 MM5204 is a 1096 bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a 50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

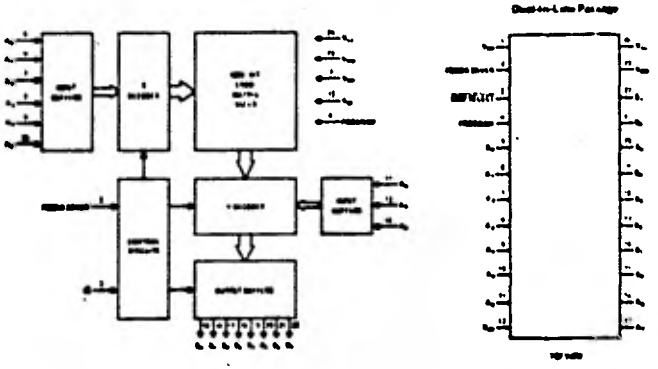
features

- Field programmable
- Fast program time: ten seconds typical for 4096 bits
- Fast access time
  - MM4204 1.25μs
  - MM5204 1μs
- DTL/TTL compatibility
- Standard power supplies: 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI STATE® output Chip Select input (CS)
- "O" quartz lid version erasable with short wave ultra violet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications

applications

- Code conversion
- Random logic synthesis
- Table look up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package

Top View

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204	0°C to +70°C
MM4204	−55°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}. MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS} −14		V_{SS} −4.2	V
V_{IH}	Input High Voltage		V_{SS} −1.5		V_{CC} +0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		V_{LL}	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		60	80	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			100	mA
I_{BB}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

ac electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}. MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204 V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C (*Figure 1*), (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, (*Figure 1*) (Note 4)			1.25	μs
t_{PS}	Power Saver Set Up Time					
	MM5204	(*Figure 1*)			1.0	μs
	MM4204	(*Figure 1*)			2.0	μs
t_{CO}	Chip Select Delay					
	MM5204	(*Figure 1*)			500	ns
	MM4204	(*Figure 1*)			600	ns
t_{OH}	Data Hold Time	(*Figure 1*)	30	50		ns
t_{DSC}	Chip Select Deselect Time					
	MM5204	(*Figure 1*)	30	300	500	ns
	MM4204	(*Figure 1*)	30	300	600	ns
t_{DSP}	Power Saver Deselect Time					
	MM5204	(*Figure 1*)	30	300	500	ns
	MM4204	(*Figure 1*)	30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{BB}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{BB}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

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programmer electrical characteristics

T_A = 25°C, V_{BB} = $\overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, (see *Figure 2*). (Note 5).

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			10	mA
I_{LLO}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{BB}	V_{BB} Load Current				50	mA
I_{DD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			200	mA
V_{IHA}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILA}	Address Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHA}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLA}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLA}	V_{BB} Low Voltage		0		0.4	V
V_{BHA}	V_{BB} High Voltage		−11.4		−12.6	V
D_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{AS}	Data and Address Set Up Time		40			μs
t_{AH}	Data and Address Hold Time		0			μs
t_{CS}	Pulsed V_{DD} Set Up Time		40		100	μs
t_{CH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_{DFA}	V_{DD} Program Address and Data Fall and Rise Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" gives conditions for actual device operation.

Note 2: Calibration is not guaranteed by periodic testing.

Note 3: Positive true input notation is used except on data inputs during programming.
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: I_{ACC} = 1300 mA ± 25% (1 where N is the number of devices wire-OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5 programming).

Note 6: The EPROM is shipped programmed with all "0's." A V_{PHP} on any data input B0–B7 will leave the stored "0's" undisturbed and a V_{PLP} on the data input B0–B7 will write a logic "1" into that location.

Note 7: Typical values are for room temperature and T_A = 25°C, unless otherwise specified.

erase specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm².

programming

The MM5204 is normally shipped in the unprogrammed state. All 4096 bits are at logic "0" state. The Electrical Programming Characteristics and Figure 2 give the conditions for programming of the device. To the operation make the device effectively become a RAM with the 512 word location selected by address inputs A0–A8. Data inputs are B0–B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{PHP} on any data input B0–B7 will leave the stored "0's" undisturbed and a V_{PLP} on any data input B0–B7 will write a logic "1" into that location.

programming (cont.)

National offers programmer options with both the IMP16 P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16 P	IMP 16P/B05
IPC-16P	IPC 16P/B05

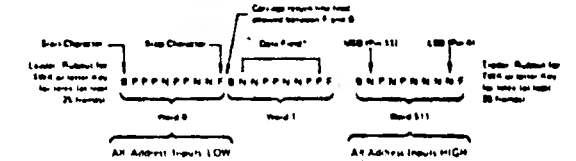
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed.

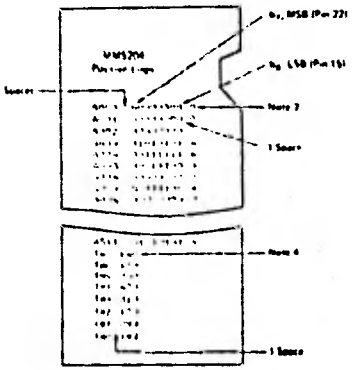
preferred format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example.



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

alternate format (Punched Tape (Note 1) or Cards)



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

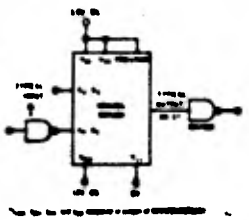
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

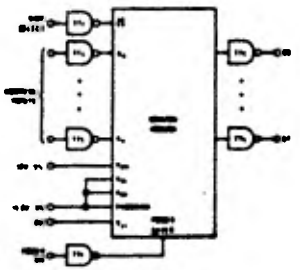
erasing procedure

The MM4204Q/MM5204Q may be erased by exposure to short wave ultraviolet light—2537 nm. There exists no absolute rule for erasing time or distance from source. The customer equipment output capability should be calculated. Establish a worst case time required with the equipment then over erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS 54 and Model S-52 manufactured by Ultra Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short wave filters. The MM4204/MM5204 should be placed about one inch away from the lamp for about 20–30 minutes.

ac test circuit



typical application



switching time waveforms

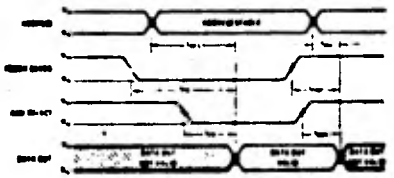


FIGURE 1. Read Operation

programming waveforms

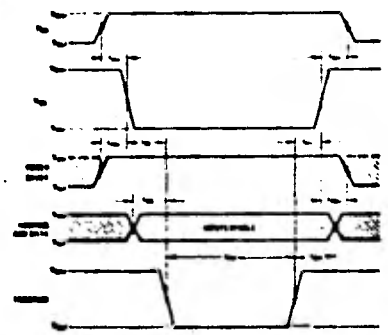
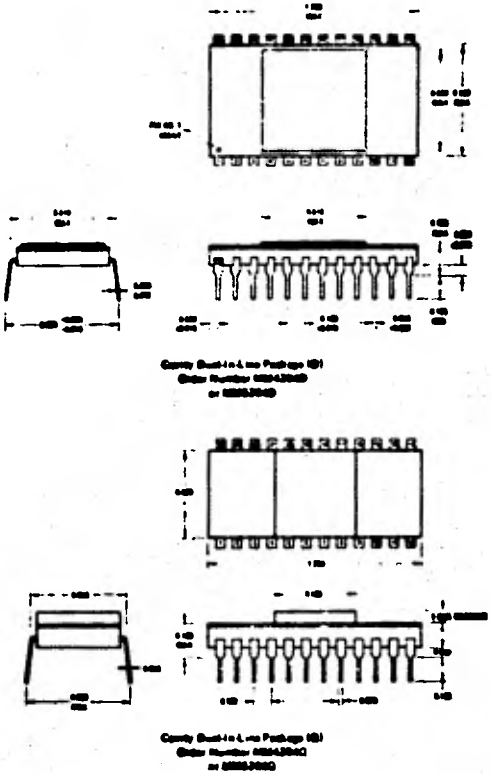


FIGURE 2. Programming Waveforms

physical dimensions



Note: A wide brazed package which meets the mechanical specifications shown above may be substituted at the discretion of the manufacturer.

National Semiconductor Corporation
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National Semiconductor (UK) Ltd.

National Semiconductor

Analog-to-Digital Converters

ADC0808, ADC0809 Single Chip Data Acquisition System

General Description

The ADC0808, ADC0809 data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any one of 8-single-ended analog signals.

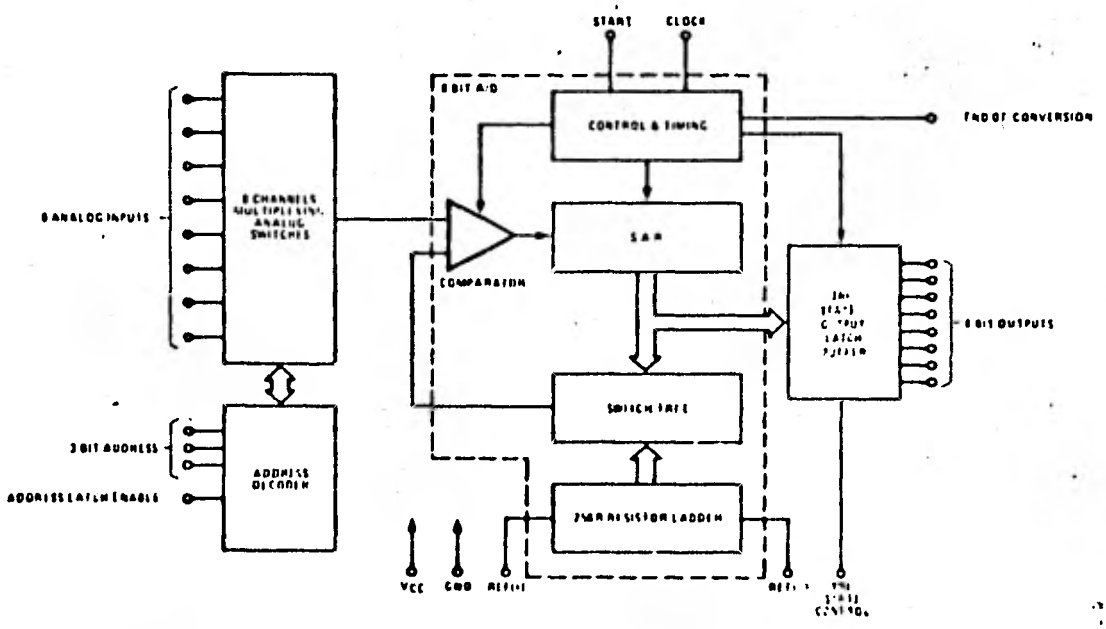
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy ≤ 1 LSB including quantizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet.

Features

- Total unadjusted error < ±1/2 LSB
- Linearity error < ±1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 μs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW
- Full −55°C to +125°C operation available

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Control Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Control Inputs (Start, TRI-STATE, Clock, ALE, ADD A, ADD B, ADD C)	−0.3V to + 15V
Operating Temperature Range	
•ADC0808CCN, ADC0809CCN	−40°C to +85°C
ADC0808CD	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (at 25°C)	500 mW
Operating V_{CC} Range	4.5V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

ADC0808CCN, ADC0809CCN
$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted, (Note 2)
ADC0808CD
$4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted, (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA @ T_A = 85°C I_O = −300 μA @ T_A = 125°C	V_{CC}−0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_D = 1.2 mA			0.45	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	Clock Frequency = 500 kHz				
		@ T_A = 85°C		300	1000	μA
		@ T_A = 125°C			3000	μA
I_{OUT}	TRI-STATE Output Current	V_O = 5V			3	μA
		V_O = 0	−3			μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to GND unless otherwise specified.

Note 3: Non-linearity error is the maximum deviation from a straight line through the end-points of the A/D transfer characteristic, *(Figure 2)*.

Note 4: Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage, *(Figure 2)*.

Note 5: Full-scale error is the difference between the output of an ideal and the actual A/D for full scale input voltage, *(Figure 2)*.

Note 6: Total unadjusted error is the maximum sum of non-linearity, zero and full-scale errors *(Figure 3)*.

Note 7: Quantization error is the ±1/2 LSB uncertainty caused by the converter's finite resolution, *(Figure 3)*.

Note 8: Absolute Accuracy describes the difference between the actual input voltage and the full scale weighted equivalent of the binary output code. Included are quantizing and all other errors. Although rarely provided on data sheets, it is the best indication of a converter's true performance, *(Figure 3)*.

Note 9: Supply rejection relates to the ability of an ADC to maintain accuracy as the supply voltage varies. The supply and $V_{REF(+)}$ are varied together and the change in accuracy is measured with respect to full scale.

Note 10: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence, *(Figure 5)*.

DC Electrical Characteristics (Continued)

ANALOG MULTIPLEXER

ADC0808CCN, ADC0809CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted.
ADC0808CD $-55°C \leq T_A \leq +125°C$ unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel)				
		$T_A = 25°C$, $R_L = 10k$		1.5	3	kΩ
		$T_A = 85°C$			6	kΩ
		$T_A = 125°C$			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10k$		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$,		10	200	nA
		$T_A = 25°C$			200	nA
		ADC0808CD @ $T_A = 125°C$			400	nA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$,	-200	-10		nA
		$T_A = 25°C$	-200			nA
		ADC0808CD @ $T_A = 125°C$	-400			nA

CONVERTER SECTION

$V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $V_{IN} = V_{COMPARATOR\ IN}$, $f_C = 640$ kHz

ADC0808CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted.
ADC0808CD $-55°C \leq T_A \leq +125°C$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/4	±1/2	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	$T_A = 25°C$ (Note 6)		±1/4	±1/2	LSB
	ADC0808CD		±1/4	±1/2	LSB
	ADC0808CCN		±1/4	±3/4	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	$T_A = 25°C$ (Note 8)		±3/4	±1	LSB
	ADC0808CD		±3/4	±1	LSB
	ADC0808CCN		±3/4	±1 1/4	LSB

ADC0809CCN $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/2	±1	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	(Note 6)		±1/2	±1	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	(Note 8)		±1	±1 1/2	LSB

ADC0808CCN $-40°C \leq T_A \leq +85°C$, **ADC0809CCN** $T_A = 25°C$
ADC0808CD $-55°C \leq T_A \leq +125°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection	$4.75V \leq V_{CC} = V_{REF(+)} \leq 5.25V$, (Note 9)		0.05	0.15	% V
Comparator Input Current	$f_C = 640$ kHz, (Note 10)	-2	±0.5	2	μA
Ladder Resistance	From $R_{ef(+)}$ to $R_{ef(-)}$	1	4.5		kΩ

DC Electrical Characteristics (Continued)

DESIGN GUIDELINES

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Voltage Across Ladder	From Ref(+) to Ref(−)	0.512	5.12	5.25	V
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder	Measured at $R_{LADDER}/2$	$\frac{V_{CC}}{2}-0.1$	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}-0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V

AC Electrical Characteristics

$T_A = 25°C$, $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{WS}	Start Pulse Width	*(Figure 5)*	200	100		ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*	200	100		ns
t_A	Address Set-Up Time	*(Figure 5)*	50	25		ns
t_H	Address Hold Time	*(Figure 5)*	50	25		ns
t_D	Analog MUX Delay Time From ALE	$R_S + R_{ON} \leq 5\ k\Omega$, $C_L = 10\ pF$		1	2.5	μs
t_{1H}, t_{H0}	TRI-STATE Control to Q Logic State	$C_L = 50\ pF$		125	250	ns
t_{1H}, t_{0H}	TRI-STATE Control to Hi-Z	$C_L = 10\ pF$, $R_L = 10k$		125	250	ns
t_C	Conversion Time	$f_C = 640\ kHz$, *(Figure 5)* (Note 11)	90	100	114	μs
f_C	Clock Frequency		10	640	1200	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	1		8	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
		At MUX Inputs		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		5	7.5	pF

Note 11: The outputs of the data register are updated one clock cycle before the rising edge of EOC.
Note 12: Capacitance guaranteed by periodic testing.

Timing Diagram

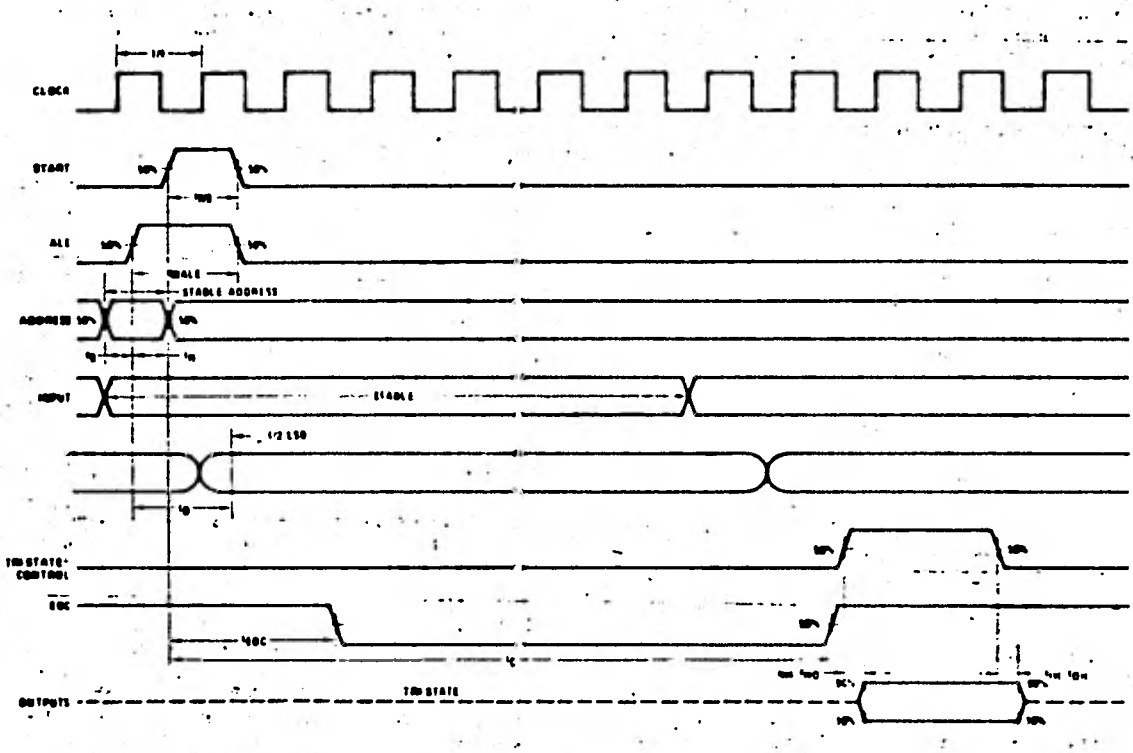


FIGURE 5

Typical Performance Characteristics

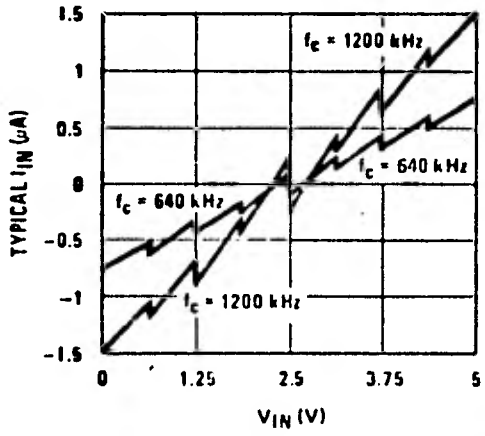


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC} = V_{REF} = 5V)

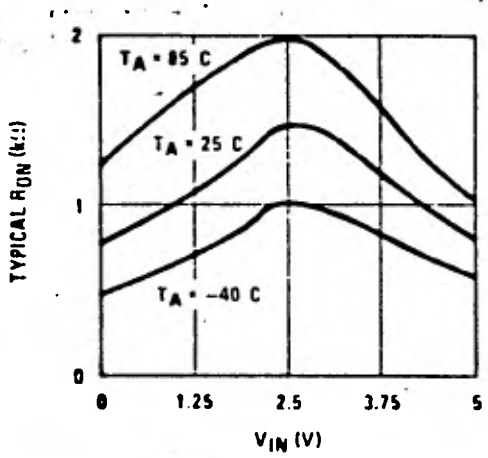


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC} = V_{REF} = 5V)

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

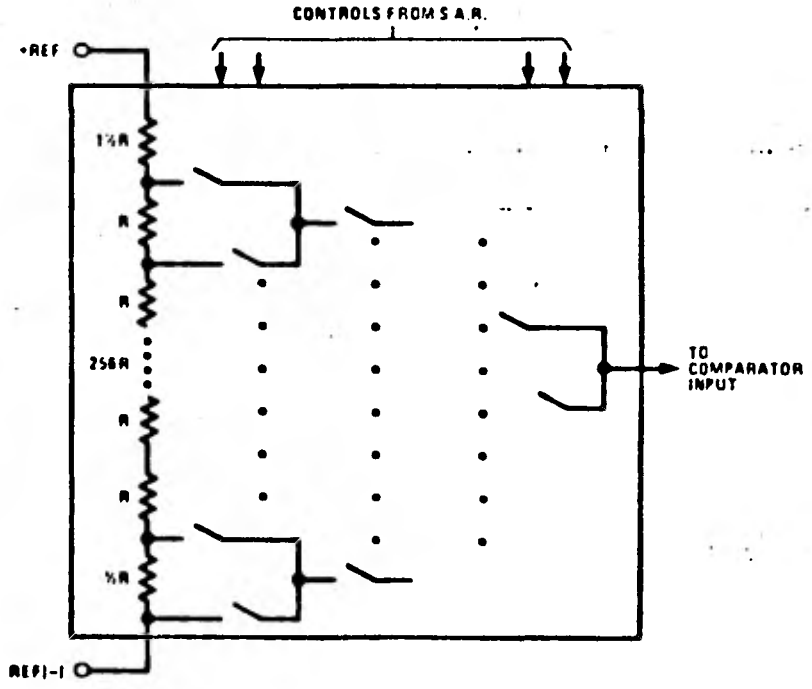


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 1 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179. The characteristic is generated with the analog input signal applied to the comparator input.

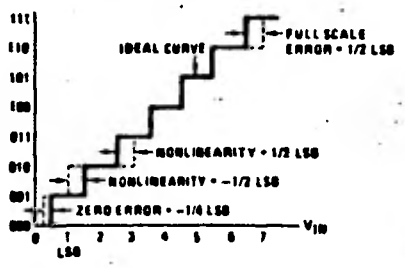


FIGURE 2. 3-Bit A/D Transfer Curve

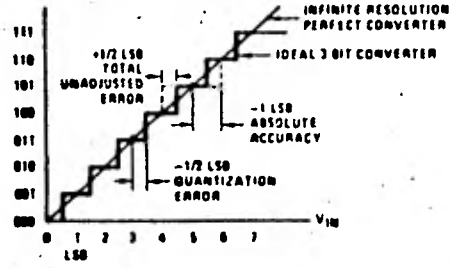


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

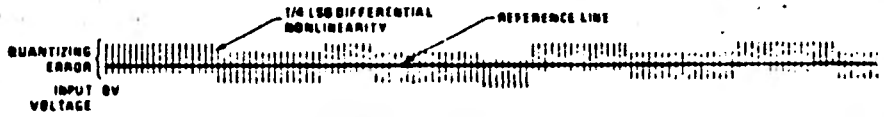
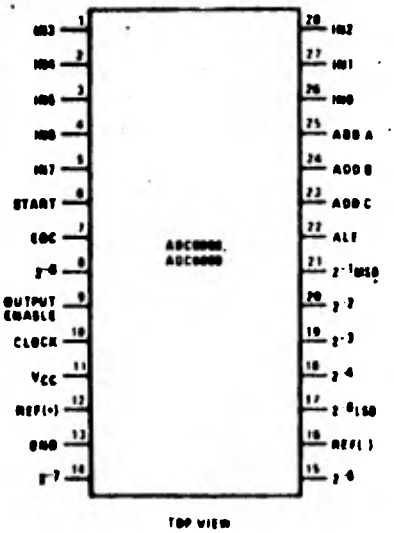


FIGURE 4. Typical Error Curve

Connection Diagrams

Dual-In-Line Package



Applications Information

OPERATION

Ratiometric Conversion

The AOC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the AOC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808
V_{fs} = Full-scale voltage
V_z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the AOC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 8)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder Ref(−) should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N channel switches to P channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 9 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 10* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 11*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 12*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

Converter Equations

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = V_{REF(+)} \left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE} \quad (2)$$

The center of an output code N is given by:

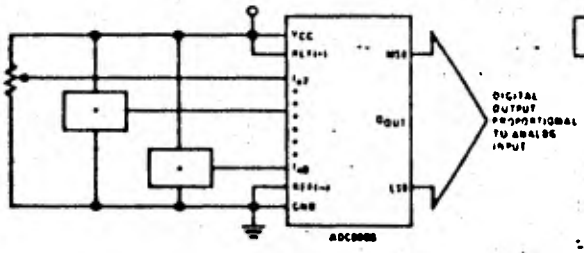
$$V_{IN} = V_{REF(+)} \left[\frac{N}{256}\right] \pm V_{TUE} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN}}{V_{REF(+)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = GND
V_{TUE} = Total unadjusted error voltage(typically $V_{REF(+)}/512$)

Applications Information (Continued)

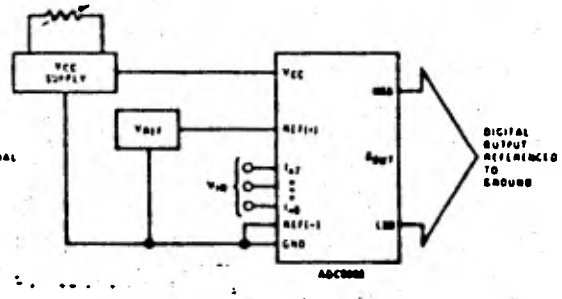


$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

*Ratiometric transducers

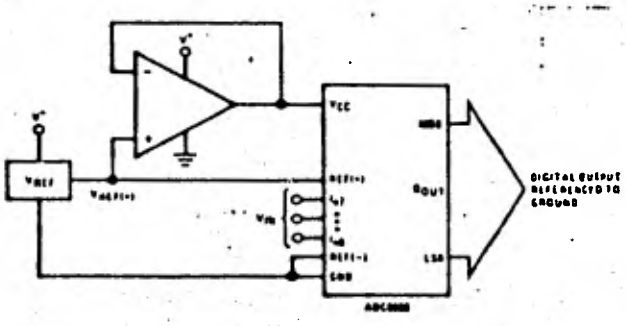
FIGURE 8. Ratiometric Conversion System



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

FIGURE 9. Ground Referenced Conversion System Using Trimmed Supply



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \le V_{CC} = V_{REF} \le 5.25V$

FIGURE 10. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

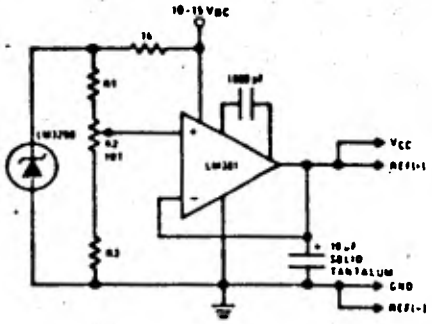
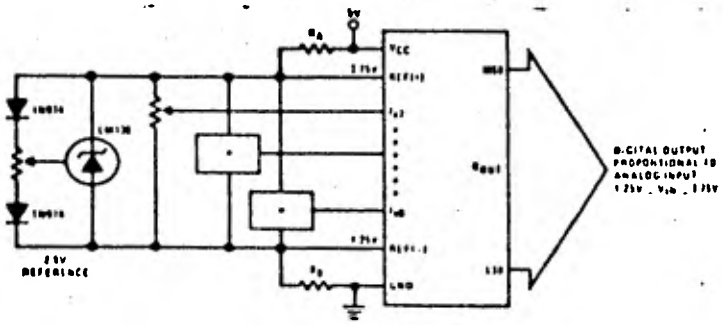


FIGURE 11. Typical Reference and Supply Circuit

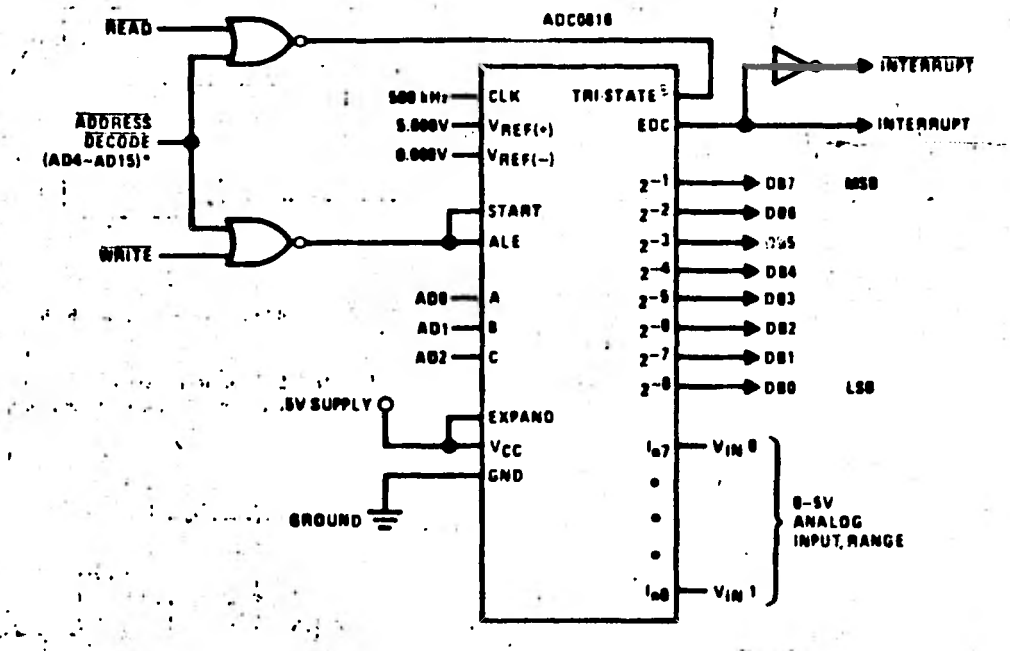


$R_A = R_B$

*Ratiometric transducers

FIGURE 12. Symmetrically Centered Reference

Typical Application



*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA · Φ2 · R/$\overline{\text{W}}$	VMA · Φ2 · R/$\overline{\text{W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

ORDER NUMBER	TEMPERATURE RANGE	25°C TOTAL UNADJUSTED ERROR	SEE NS PACKAGE NUMBER
ADC0808CD	−55°C to +125°C	±1/2 LSB	D28A
ADC0809CCN	−40°C to +85°C	±1/2 LSB	N28A
ADC0809CCN	−40°C to +85°C	±1 LSB	N28A

APENDICE B

-Listado programa CONPLU I

-Listado programa RAP-AIM-65-VIII

CONPLO 1

ESTE PROGRAMA HA SIDO DISE&ADO PARA EL MICROPROCESADOR SC/MP. CUENTA LOS EVENTOS PROVENIENTES DE UN PLUVIOMETRO TIPO BALANCIN, Y ESTA SUMA LA ALMACENA EN UNA LOCALIDAD DE MEMORIA(F03). LA RUTINA PRINCIPAL ES UN RELOJ QUE PROPORCIONA LAS MARCAS DE TIEMPO(10 MIN.) PARA EL ENVIO DE DATOS DE LA ESTACION DE CAMPO HACIA UNA ESTACION RECEPTORA. AL INICIARSE LA TRANS, EL PROGRAMA ENCIENDE EL TRANSMISOR,ENVIA EL BLOQUE DE INFORMACION Y APAGA EL TRANSMISOR PARA INICIAR UN NUEVO PERIODO DE TRANSMISION. EL BLOQUE DE INFORMACION CONSISTE EN ENVIAR PRIMERO EL IDENTIFICADOR DE LA ESTACION Y LUEGO LA PRECIPITACION PLUVIAL ACTUAL SEGUIDA DE LAS TRES PRECIPITACIONES ANTERIORES, PARA ASI EVITAR LA PERDIDA DE INFORMACION.

PROGRAMA PRINCIPAL
PRIMERA PARTE

```
0000  08          NOP
0001  06          CSA                    ;RESET\F/F
0002  DC02        ORI  02
0004  07          CAS
0005  C4CB        LDI
0007  BF04        DLY  5 MS
0009  06          CSA
000A  D4FD        ANI  FD
000C  07          CAS
000D  C402        LDI                    ;APUNTADOR MEMORIA RAM
000F  32          XPAL
0010  C40F        LDI
0012  36          XPAH
0013  06    $IMDA CSA                    ;TRANSMISION MANUAL?
0014  D420        ANI  20
0016  9C27        JNZ  $TRANSMISION
0018  C48D $INICIO LDI                   ;SUBRUTINA DE INTERRUPCION
001A  33          XPAL                   ;EN EL P3
001B  C400        LDI
001D  37          XPAH
001E  C400        LDI                    ;PRECIP. ACUM.=0
0020  CA01        ST    P2+1
0022  05          IEN                    ;SE INICIA PERIODO DE
0023  C40A        LDI 0AHEX  CONTA1      ;TRANSMISION
0025  CA07        ST    P2+7
0027  C41E  $L3    LDI   CONTA2
0029  CA08        ST    P2+8
002B  C40A  $L2    LDI   CONTA3
002D  CA09        ST    P2+9
002F  C487  $L1    LDI
0031  BFC2        DLY
0033  BA09        DLD   CONTA3-1
0035  9CF8        JNZ   $L1
0037  BA08        DLD   CONTA2-1
0039  9CF0        JNZ   $L2
003B  BA07        DLD    CONTA1-1
003D  9CE8        JNZ   $L3
```

SEGUNDA PARTE

```
003F  04 $TRANS   DINT            ;ACTIVA TRANSMISOR
0040  C4FF       LDI
0042  01          XAE
0043  19          SIO
0044  C402       LDI                   ;RETARDO DE UN SEGUNDO
0046  CA06       ST
0048  C4AB  $L6   LDI
004A  33          XPAL
004B  C400       LDI
004D  37          XPAH
004E  3F          XPPC $1/2SEG
004F  BA06       DLD
0051  9CF5       JNZ  $L6
0053  C4B8       LDI                   ;INFAIR EN P3
0055  33          XPAL
0056  C400       LDI
0058  37          XPAH
0059  C4E0       LDI                   ;IDENTIFICADOR ESTACION
005B  3F          XPPC $INFAIR          ;TRANSMITE IDENTIFICADOR
005C  C403       LDI                   ;STACK DE INFORMACION EN P1
005E  31          XPAL
005F  C40F       LDI
0061  35          XPAH
0062  C405       LDI  CUNTA4           ;CONTADOR DE DATOS
0064  CA06       ST
0066  C4AB   $L4  LDI
0068  33          XPAL
0069  C400       LDI
006B  37          XPAH
006C  3F          XPPC $1/2SEG
006D  BA06       DLD
006F  9808       JZ   $CONTINUA
0071  C4B8       LDI                   ;INFAIR EN P3
0073  33          XPAL
0074  C400       LDI
0076  37          XPAH
0077  C501       LD   P1+1 @
0079  3F          XPPC $INFAIR
007A  90EA       JMP  $L4
007C  C400 $CONTINUALDI                 ;DESACTIVA TRANSMISOR
007E  01          XAE
007F  19          SIO
0080  C404       LDI  CUNTA5           ;REACOMODO DE DATOS
0082  CA06       ST
0084  C5FF   $L5  LD   P1-1@
0086  C901       ST   P1+1
0088  BA06       DLD  CUNTA5-1
008A  9CFB       JNZ  $L5
008C  908A       JMP  $INICIO
```

SUBRUTINA DE INTERRUPCION

```
008E  CA05 $INT   ST P2+5               ;GUARDA ACUMULADOR EN MEMORIA
0090  06          CSA                   ;RESET F/F ALTO
0091  DC02       ORI
0093  07          CAS
0094  C4E1       LDI
0096  8F0A       DLY
0098  AA01       ILD                   ;PRECIP. ACUM.+1
009A  33          XPAL                  ;SALVA LA DIRECCION DONDE FUE
009B  31          XPAL                  ;INTERRUMPIDO EL PROGRAMA
009C  37          XPAH                  ;PRINCIPAL
009D  35          XPAH
009E  C4BD       LDI                   ;DIRECCION DE INTERRUPCION
```

```
00A0  33            XPAL                ;EN P3
00A1  C400          LDI
00A3  37            XPAH
00A4  06            CSA                 ;RESET F/F BAJO
00A5  D4FD          ANI
00A7  07            CAS
00A8  C205          LD                  ;SE REINTEGRA DATO DEL ACUMULADOR
00AA  05            IEN                 ;SE ACEPTA INTERRUPCION
00AB  3D            XPPC                ;RETORNA


          1/2 SEG SUBRUTINA

00AC  C405 $1/2SEG  LDI CONTA6
00AE  CA0A          ST
00B0  C440   $L7    LDI                 ;RETARDO DE 0.1 SEG.
00B2  BFB1          DLY
00B4  BA0A          DLD  CONTA6-1
00B6  9CFB          JNZ  $L7
00B8  3F            XPPC                ;RETORNA


          INPAIR
SUBRUTINA DE ENVIO DE DATOS EN SERIE.
EMPIEZA CON EL BIT MENOS SIGNIFICATIVO.

00B9  01    $INPAIR XAE                 ;DATO EN EL EXTENSION REGISTER
00BA  C4FF          LDI
00BC  BF17          DLY
00BE  06            CSA
00BF  DC01          ORI
00C1  07            CAS
00C2  C409          LDI
00C4  CAFF          ST    P2-1
00C6  C481    $L8   LDI
00C8  BF0B          DLY
00CA  BAFF          DLD
00CC  9B10          JZ    $SALIDA
00CE  40            LDE
00CF  D401          ANI
00D1  CAFE          ST    P2-2
00D3  01            XAE                 ;CORRIMIENTO DEL BIT (1) AL
00D4  1C            SR                  ;BIT (1-1)
00D5  01            XAE
00D6  06            CSA
00D7  DC01          ORI
00D9  E2FE          XOR   P2-2
00DB  07            CAS                 ;TRANSMITE BIT INFORMACION
00DC  90E8          JMP   $L8
00DE  06    $SALIDA CSA                 ;PONE STOP BIT (ALTO)
00DF  D4FE          ANI
00E1  07            CAS
00E2  3F            XPPC                ;RETORNA
R
```

RAP-AIM-65-V111

REGISTRO AUTOMATICO DE PRECIPITACION;ENLACE TELEMETRICO EXPERIMENTAL PARA ADQUISICION REMOTA DE DATOS HIDROLOGICOS. LOS DATOS SE RECIBEN EN FORMA ASINCRONA: IDENTIFICADOR DE ESTACION ID,PRECIPITACION ACUMULADA PO,PRECIPITACIONES ACUMULADAS DE PERIODOS ANTERIORES R-1, R-2 Y R-3. EL IDENTIFICADOR DE ESTACION ESTA PROGRAMADO COMO HEX E0 (1110 0000). PERIODM DE TRANSMISION 10 MIN. TMAX PARA RECIBIR DATOS 15 MIN. TABU PARA ABORTO SI NO LLEGAN DATOS: 1 HORA. TMAX Y TABU SE FIJAN EN LAS LOCALIDADES <0087>-<008A>. EL IDENTIFICADOR SE PUEDE CAMBIAR EN LA LOCALIDAD <0483> Y LOS DATOS RECIBIDOS COMPLEMENTAR EN <047A>. EL NUMERO DE DATOS POR TRANSMISION SE SELECCIONA EN <0496>. EL PROGRAMA SE ESCRIBIO EN FAM, 2K DE MEMORIA.

```
010C            JMP 0000            ;DEFINE FUNCION F1

0000  START     NOP
0001            NOP
0002            NOP
0003            NOP
0004            NOP
0005            JSR CRLF(E9F0)      ;ENABLE PRINTER
0008            LDA #80
000A            STA A411
000D            LDA #00             ;IMPRIME "FECHA?-"
000F            STA TEXTO(92)
0011            LDX #07
0013            JSR PRINT(02BB)
0016            LDX #00
0018    G01     JSR RDKUP(E95F)     ;ENTRADA TECLADO DE LA FECHA
001B            STA 80,X            ;(9 CARACTERES) JUN-02-80
001D            INX
001E            CPX #09
0020            BMI G01
0022            JSR CRLF (E9F0)     ;NUEVO RENGLON
0025            LDA #07             ;IMPRIME "HORA?-"
0027            STA TEXTO
0029            LDX #0D
002B            JSR PRINT
002E            LDX #00             ;ENTRADA TECLADO DE LA HORA
0030    G02     JSR RDKUP           ;(8 CARACTERES)
0033            STA A5,X            ;H1OH1:M1OM1:S1OS1
0035            INX
0036            CPX #08
0038            BMI G02
003A            JMP SIGUE

020A    SIGUE   JSR CRLF            ;DEFINE VECTOR DE INTERRUPCION
020D            LDA #INT-L
020F            STA A400
0212            LDA #INT-H
0214            STA A401
0217            LDA #30             ;LI=0 CONTADOR INTERRUPCIONES
0219            STA 9A              ;POR SEGUNDOS
021B            NOP
021C            NOP
021D            LDA #00            ;PUERTO A= ENTRADAS
021F            STA A003(DDRA)
```

```
0222            STA 0000(URB)           ;PUERTO B=00
0225            LDA #FF                 ;PUERTO B= SALIDAS
0227            STA A002
022A            LDA #3D                 ;INHIBE TODAS LAS INTERRUPCIONES
022C            STA A00E                ;EXCEPTO T1 Y CA1
022F            LDA #C2                 ;HABILITA LAS INTERRUPCIONES T1 Y CA1
0231            STA A00E
0234            LDA #41                 ;INTERRUP. CONTINUA EN T1,PB7 DESHA-
0236            STA A00B                ;BILITADO,PUERTO A LATCH CUANDO CA1
0239            LDA #01                 ;SET IFR1 CON SUBIDA DE CA1
023B            STA A00C
023E            LDA A001                ;BORRA BANDERA DE INTERRUPCION CA1
0241            LDA #00                 ;ESCRIBE EN LA PARTE BAJA DEL LATCH
0243            STA A006
0246            LDA #F4                 ;ESCRIBE F400HEX EN EL CONTADOR
0248            STA A005              ;RESET BANDERA INTERRUPCION T1
0250            LDA #13                 ;IMPRIME "PREC.TOT.AC.?"
0252            STA TEXTO
0254            LDX #22
0256            JSR PRINT
0259            JSR RD2                    ;ENTRADA TECLADO PTA1000 Y PTA100
025C            STA 99                  ;Y CONVERSION A 2 BYTES BCD
025E            JSR RD2                 ;ENTRADA TECLADO PTA10 Y PTA
0261            STA 98                  ;Y CONVERSION A 2 BYTES BCD
0263            JSR CRLF                ; NUEVO RENGLON
0266            LDA #00
0268            STA BC                  ;PF=0
026A            STA BE                  ;CF=0
026C            STA 91                  ;CS=0
026E            STA 90
0270            STA 88                   ;TOG=0
0272            LDA #01                 ;CE=1
0274            STA 8D
0276            JSR 0280   ASTRIX
0279            JSR E9F0   CRLF
027C            JMP 02E0   DADRE

        SUBRUTINA IMPRIME 20X "*"

0280  ASTRIX   LDA #00
0282   G03     LDA #2A
0284            JSR E97A   OUTPUT
0287            INX
0288            CPX #14
028A            BNE 0282   G03
028C            RTS

         SUBRUTINA IMPRIME FECHA Y HORA

0290   PRTFH   LDX #00                  ;IMPRIME LA FECHA
0292     G04   LDA 9C,X
0294           JSR E97A   OUTPUT
0297           INX
0298           CPX #09
029A           BMI 0292   G04
029C           JSR E83B                 ;3 ESPACIOS
029F           JSR E83E
02A2           LDX #00                ;IMPRIME LA HORA
02A4         G05  LDA A5,X
02A6           JSR E97A   OUTPUT
02A9           INX
02AA           CPX #08
02AC           BMI 02A4   G05
02AE           RTS
```

```
          SUBRUTINA IMPRIME TEXTO

0288   PRINT  LDA TOP,X(3D)
028A          JSR E9BC  OUTALL
028D          DEX
028E          CPX 92    TEXTO
02C0          BNE 0288  PRINT
02C2          RTS


          SUBRUTINA CONVERSION A BCD DE DATO HEX EN A Y
          LO DEJA CONVERTIDO EN A (MAX. #BCD=99=63HEX)

02C5          NOP
02C6          NOP
02C7          BEQ 02D5  HECHO
02C9          TAX                    ;CONVIERTE DATO HEX A BCD
02CA          SED
02CB          LDA #00
02CD    OTRO  DEX
02CE          CLC
02CF          ADC #01
02D1          CPX #00
02D3          BNE 02CD  OTRO
02D5    HECHO RTS

02E0    DAORE LDA 8C                 ;PF=0? SI PF=1 PROCESA DATOS
02E2          BEQ 02F6  DISPFH
02E4          JMP 039D  PROCES

02F6   DISPFH LDA #00               ;DISABLE PRINTER
02F6          STA A411
02FB          JSR EB44  CLR          ;CLEAR D/P PRINTER
02FE          JSR 0290  PRTFH        ;DESPLEGA FECHA Y HORA
0301          JMP 0330  NEWSEG


0330   NEWSEG LDA AC                 ;CAMBIO SEGUNDO?
0332          STA 8F
0334    GOB   LDA AC
0336          CMP 8F
0338          BEQ 0334  GOB
033A          NOP
.
.
.
.
0341          LDA 91                 ;CONMUTA PB0 SI TOG=1
0343          AND 88 (TOG)           ;ALARMA INTERMITENTE DE 1 SEG.
0345          STA A000  (ORB)
0348          NOP
0349   INCSEG SED                    ;CS=CS+1 (CS SON 2 DIGITOS BCD)
034A          CLC
034B          LDA #01
034D          ADC 91
034F          STA 91
0351          LDA #00
0353          ADC 90
0355          STA 90
0357    CE    LDA 8D               ;CE=1?
0359          BEQ 0385  CSTABO

035E  CSTMAX  LDA 87                 ;CS>TMAX?
0360          CMP 90
0362          BCC 036F  NODAT        ;SI CS>TMAX ->NODAT
```

```
0364            BNE 037A   G09
0366            LDA 88                  ;SI CS < TMAX->DAORE
0368            CMP 91
036A            BCS 037A   G09

036F   NODAT    JSR 0440   PRTNDAT      ;IMPRIME "NO LLEGARON DATOS",
0372            LDA #01                 ;ACTIV ALARMA INTERMITENTE
0374            STA 88 (TOG)            ;TOG=1
0376            LDA #00                 ;CE=0
0378            STA 8D
037A      G09   JMP 02E0   DAORE

0385  CSTABO   LDA 89                  ;CS>TABO?
0387            CMP 90
0389            BCC 0393   ABORT        ; SI CS>TABO->ABORT
038B            BNE 037A   G09 .
038D            LDA 8A                  ;SI CS<TABO->DAORE
038F            CMP 91
0391            BCS 037A   G09
0393            JMP 0545   PRTFALLA     ;IMPRIME FALLA DE TRANSMISION"
                                         FECHA Y HORA,ENCIENDE TONO Y ABORTA

039D  PROCES    NOP
.
.
.

03A2  PREC0     LDA 94                  ;PREC=0?
03A4            BNE 0430   PRTDATA
03A6            JMP 0426   SAL
03A9  PRTDAT    JSR 0430   PRTAST       ;IMPRIME ASTERISCOS

03AE  LLUVIA    NOP
03AF            NOP
03B0            NOP
03B1            JSR 0290   PRTFH         ;IMPRIME FECHA Y HORA
03B4            JSR EA13   CRLOW
03B7            LDA #0E                 ;IMPRIME "EST.-"
03B9            STA 92     TEXTO
03BB            LDX #12
03BD            JSR 0288   PRINT
03C0            LDA #49                 ;IMPRIME "I1".(DEFINE EL # DE
03C2            JSR E9BC   OUTALL       ;ESTACION O TIPO CORRESPONDIENTE
03C5            LDA #49                 ;AL CODIGO ID ENVIADO DE LA ESTACION
03C7            JSR E9BC   OUTALL
03CA            JSR E83B                ;5 ESPACIOS
03CD            JSR E83B
03D0            JSR E83B
03D3            LDA #1D                 ;IMPRIME"PREC."
03D5            STA 92     TEXTO
03D7            LDX #22
03D9            JSR 0288   PRINT
03DC            JSR E83E                ;ESPACIO
03DF            LDA 94                  ;IMPRIME DATO Y CONVIERTE DE HEX
03E1            JSR 02C5   IBCD         ;A BCD E IMPRIME
03E4            STA 94
03E6            JSR EA46   NUMA
03E9            JSR EA13   CRLOW        ;NUEVO RENGLON
03EC            NOP
.
.
.
03F1            LDA #14                 ;IMPRIME "PREC.TOT.ACUM"
03F3            STA 92     TEXTO
03F5            LDX #22
```

```
03F7          JSR 0288  PRINT
03FA          JSR E838                ;2 ESPACIOS
03FD          NOP
.
.
.
0400          CLC                     ;BORRA ACARREO
0401          SED                     ;MODO DECIMAL
0402          LDA 94    PREC          ;PREC.TOT.AC.+PREC.
0404          ADC 98
0406          STA 98
0408          LDA #00
040A          ADC 99
040C          STA 99
040E          JSR EA46  NUMA
0411          LDA 98
0413          JSR EA46  NUMA          ;IMPRESION DE LA NUEVA PREC.TOT.AC.
0416          JSR E9F0  CRLF
0419          NOP
.
.
.
041E   SAL    LDA #00                 ;PF=0
0420          STA 8C
0422          JMP 02E0  DAORE

          SUBRUTINA PRENDE IMPRESORA E IOMPRIME RENGLON ASTERISCOS

0430  PRTAST  LDA #80                  ;PRENDE IMPRESORA
0432          STA A411
0435          JSR EB44  CLR
0438           JSR 0280  ASTRIX       ;RENGLON ASTERISCOS
0438         JSR EA13  CRLOW0
043E          RTS

          SUBRUTINA IMPRIME "NO LLEGARON DATOS FECHA Y HORA"

0440  PRINDAT JSR 0430  PRTAST
0443          LDA #37                 ;IMPRIME "NO LLEGARUN DATOS!"
0445          STA 92    TEXTO
0447          LDX #49
0449          JSR 0288  PRINT
044C          JSR EA13  CRLOW
044FJSR 0290  PRTFH                   ;IMPRIME FECHA Y HORA
0452          JSR EA13  CRLOW
0455          RTS


0460    INT   PHA                     ;A->STACK
0461          PHP                     ;PS->STACK
0462          TXA
0463          PHA                     ;X->STACK
0464          TYA
0465          PHA                     ;Y->STACK
0466          NOP
.
.
.
0468          LDA #02                 ;HUBO INTERRUPCION POR RELOJ(Z=1)
046D          AND A00D  IFR           ;O DATOS (Z=0)
0470          BEQ 0488  INTCLK
0472          NOP
.
.
```

```
0475  INTDAT  INC 8E     CF          ;CF=CF+1
0477          LDA A001   ORA          ;LEE PUERTO A,BORRA CAI
047A          NOP                    ;AQUI SE PUEDEN COMPLEMENTAR LOS
047B          NOP                     ;DATOS EOR #FF
047C          TAY                     ;A(DSATO)->Y
047D          LDX #01                 ;CF=1?
047F          CPX 8E
0481          BNE 0493   MEMDAT
0483   IDOK   CPY #2A                 ;ID=2A?
0485          BNE 04A0   CFO
0487          LDA #01                 ;CE=1
0489          STA 8D
048B          LDA #00
048D          STA 90                  ;C S=0
048F          STA 91
0491          STA 88                 ;TOG=0 APAGA ALARMA
0493  MEMDAT   TYA                     ;Y(DATO)->MEMORY (CF),ALMACENA
0494          LDX 8E     (CF)         ;DATO LEIDO
0496          STA 92,X
0498   CFMAX  CPX #02                 ;CF=CFMAX?,SI NO SALINT
049A          BNE 04A4   SALINT
049C          LDA #01                 ;PF=1 IMPRIME DATOS YA QUE SE
049E          STA 8C                  ;RECIBIERON TODOS
04A0          LDA #00                 ;CF=0
04A2          STA 8E
04A4  SALINT  JMP 052F   SALINT


04B8  INTCLK  INC 9A                  ;C1=CU=1
04BA          LDX #40                 ;C1=16? (1SEG?)
04BC          CPX 9A
04BE          BNE 0520   SALINT
04C0          LDA #30                 ;C1=0  (30 ASCII)
04C2          STA 9A
04C4          NOP
.
.
.

04C7SECUNDERO INC AC                 ;S1=S1+1
04C9           LDX #3A                ;S1=10?
04CB          CPX AC
04CD          BNE 0520   SALINT       ;SAL SI S1 DIF. DE 10
04CF          STA AC                  ;S1=30
04D1          INC AB                  ;S10=S10+1
04D3          LDX #36
04D5          CPX AB                  ;S10=6?
04D7          BNE 0520   SALINT
04D9          LDA #30                 ;S10=30
04DB          STA AB
04DD MINUTERO INC A9                  ;M1=M1+1
04DF          LDX #3A
04E1          CPX A9                  ;M1=10?
04E3          BNE 0520   SALINT
04E5          STA A9                  ;M1=30
04E7          INC A8                  ;M10=M10+1
04E9          LDX #36                 ;M10=6?
04EB          CPX A8
04ED          BNE 0520 SALINT
04EF          STA A8                 ;M10=30
04F1 CIAHORAS INC A6                  ;H1=H1+1
04F3          LDX #3A
04F5          CPX A6                  ;H1=10?
04F7          BNE 0500   NUDAY
04F9          STA A6                  ;H1=30
```

```
04FB            INC A5                  ;H10=H10+1
04FD            JMP 0520  SALINT
      0500  NUDAY   LDX #34                   ;H1=4?
0502            CPX A6
0504            BNE 0520  SALINT
0506            LDX #32                 ;H10=2?
0508            CPX A5
050A            BNE 0520  SALINT
050C            STA A5                  ;H10=30 YA QUE SE ACUMULARON
050E            STA A6                  ;H1=30   24 HORAS
0510 CTADIAS    INC A1                  ; D1=D1+1
0512            LDX #3A
0514            CPX A1                  ;D1=10?
0516            BNE 0520  SALINT        ;SAL SI D1 DIF. 10
0518            STA A1
051A            INC A0                  ; D10=D10+1
051C            NOP
.
.
.
0520  SALINT  PLA                       ;A<-STACK
0521            TAY                     ;A->Y
0522            PLA                     ;A<-STACK
0523            TAX                     ;A->X
0524            PLP                     ;PS<-STACK
0525            LDA A004                ;BORRA BANDERA DE INTERRUPCION T1
0528            PLA                     ;A<-STACK
0529            RTI
052A            NOP
.
.
.
0530 PRTFALLA JSR 0430  PRTAST          ;IMPRIME "FALLA DE TRANSMISION"
0533            LDA #23
0535            STA TEXTO
0537            LDX #37
0539            JSR PRINT
053C            JSR CRLDW
053F            JSR PRTFH               ; IMPRIME FECHA Y HORA
0542            JSR CRLDW
0545            JSR ASTRIX
0548            JSR ASTRIX
054B            JSR EA13
054E   FIN      LDA #01                 ;ENCIENDE ALARMA
0550            STA A000 ORB            ;TONO PERMANENTE
0553            LDA #00                 ;APAGA IMPRESORA
0555            STA A411
0558            JSR CLR
055B            LDA #23                 ;DESPLEGA "FALLA DE TRANSMISION"
055D            STA TEXTO
055F            LDX #37
0561            JSR PRINT
0564   LOOP     NOP
0565            NOP                     ;LOOP FINAL DEJA LETRERO EN EL DISPLAY
0566            JMP LOOP
0569            NOP
R
```